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Integrated sound intercarrier amplifier and transformerless audio stage for colour tv receiver

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Mullard Central Application Laboratory

UDC 621.397.132:621.375.4.029.55—419.7[681.84]

The application of the TAA570 integrated circuit in the intercarrier sound system of television receivers is described. The integrated circuit is encapsulated in a 10-lead TO-74/SOT-14 envelope. It includes the functions of amplification and limiting of the f.m. 6MHz intercarrier sound signal, subsequent demodulation, and audio pre-amplification with provision for a remote d.c. volume control. The TAA570 offers considerable simplification of the external circuitry, and requires only very simple alignment. The high sensitivity and good a.m. rejection ensure that the sound channel is free from intercarrier buzz over a wide range of receiver tuning.

INTRODUCTION

A block diagram of the intercarrier sound system using a TAA570 is shown in Fig. 1. The 6MHz intercarrier sound signal derived from the sound detector is fed through a bandpass filter to the input of the TAA570. The detector requires a 6MHz LC tuned circuit. The audio output level may be adjusted by a remote d.c. control, and is sufficient to directly drive an output stage using a PCL86 or a transistor amplifier of suitable sensitivity.

TAA570 INTEGRATED CIRCUIT

Amplification and limiting

Four differential stages of limiting are employed, using constant-current driven long-tailed pairs. The circuit is arranged so that the transistors are not driven into saturation, thus keeping spurious phase and pulse-width modulation to a minimum.

Detection

Demodulation of the f.m. signal is achieved with a full-wave gated coincidence, or quadrature, detector. The relevant circuit is shown in Fig. 2.

Operation of the circuit is seen by reference to the idealised waveforms in Fig. 3. The square-wave output V_1 of the limiters is compared with a sinusoidal reference signal V_2 which is phase shifted by 90°, obtained via an integrated capacitor and the external LC tuned circuit. Current pulses are available for the load R_L alternately from the collectors of TR_{21} and TR_{24}. The width of the output pulses is equal to the phase difference Φ between V_1 and V_2. In addition to providing the initial 90° phase-shift, the LC circuit also provides a deviation in the relative phase-shift between V_1 and V_2 as the instantaneous frequency is shifted. Thus, with V_1 frequency modulated, the collector current I_L will be pulse-width modulated, and the modulation may be derived from the average current output. The output is integrated by R_L and C_D, these components also providing the necessary de-emphasis.

Amplitude modulation of the 6MHz intercarrier may give rise to asymmetry in the square-wave output of the limiters. It is shown in Fig. 3 that an assymmetry δ in V_1 will alternately add and substract from the output current pulses; thus full-wave operation results in a high degree of pulse-width cancellation, maintaining good a.m. rejection. The excellent matching characteristics of integrated components ensure consistent cancellation. In addition, the combination of a fully balanced limiting and detection system greatly reduces a.f. disturbances in the output under impulse interference conditions.

Full-wave operation also gives the advantage that the fundamental component of the output current is 12MHz, the 6MHz intercarrier being absent; thus the overall stability is improved.

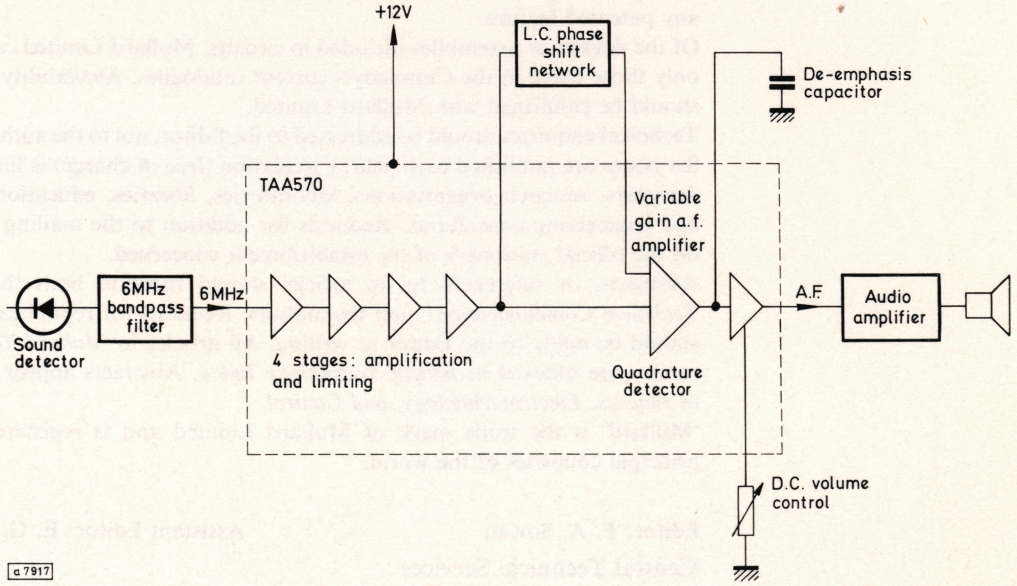

Fig. 1—Block diagram of television sound circuit using the TAA570

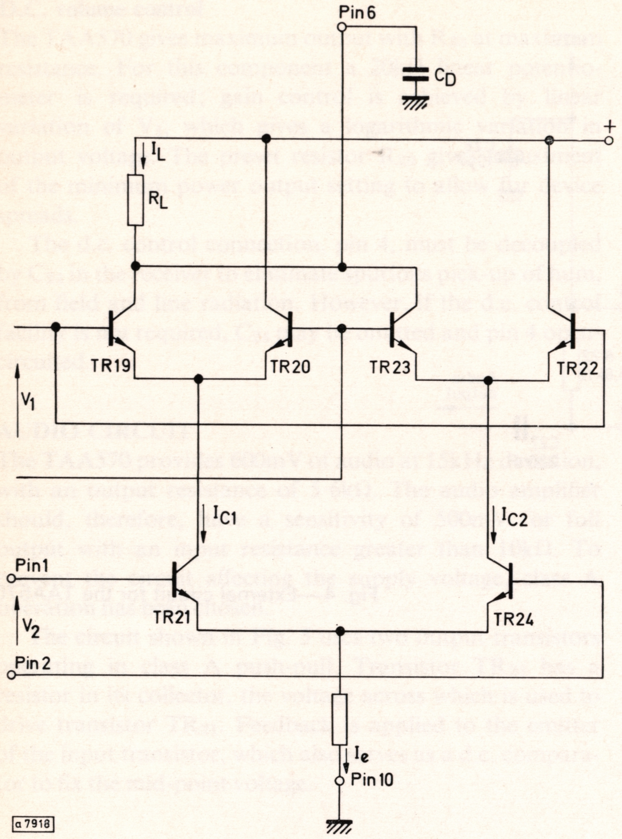

Fig. 2—Quadrature detector (Part of integrated circuit)

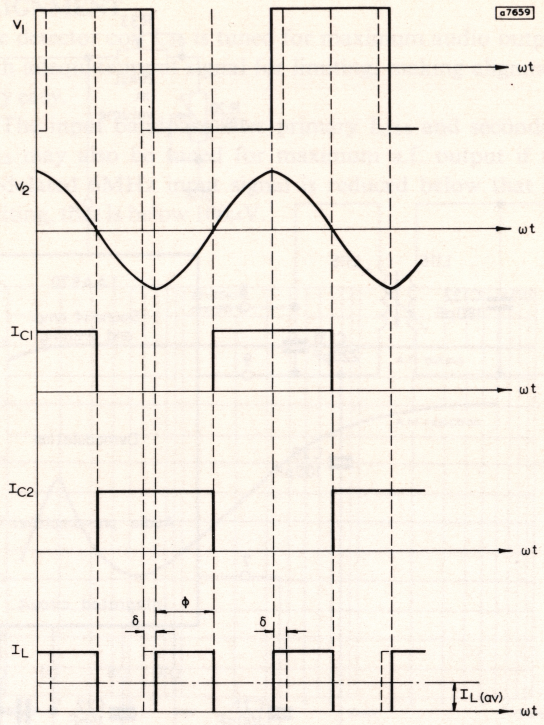

Fig. 3—Detector waveforms

Audio stages

The audio output from the detector is fed to a long-tailed pair. The audio output of the integrated circuit is taken from the collector of a transistor; control of the base bias to this transistor varies the current sharing between the transistors forming the long-tailed pair, and consequently controls the output level. A control range of greater than 60dB is available.

TAA570 EXTERNAL CIRCUIT

The external circuit used with the TAA570 is shown in Fig. 4. The integrated circuit requires a +12V supply at approximately 20mA. When used in the actual receiver, the integrated circuit is supplied, for convenience, from a +20V line via a 390Ω resistor. The value of the decoupling capacitor C_{26} is then changed to 80μF.

Layout

It is advisable to arrange the layout so that the capacitors C_{20}, C_{21}, C_{22}, and C_{23} are returned to a low-inductance chassis point close to the substrate connection, pin 10.

Input coupling

The coupling bandpass filter is designed to provide appropriate matching and selectivity between the sound detector and the input of the TAA570. The transformer shown is suitable for connection to the sound detector of the i.f. amplifier described in Ref. 1.

LC circuit

The 6MHz circuit L_{20} C_{25} has a working Q-factor chosen for a compromise between output voltage and distortion. A loaded Q-factor of 25 is considered optimum. In practice, a damping resistor R_{21} may be required.

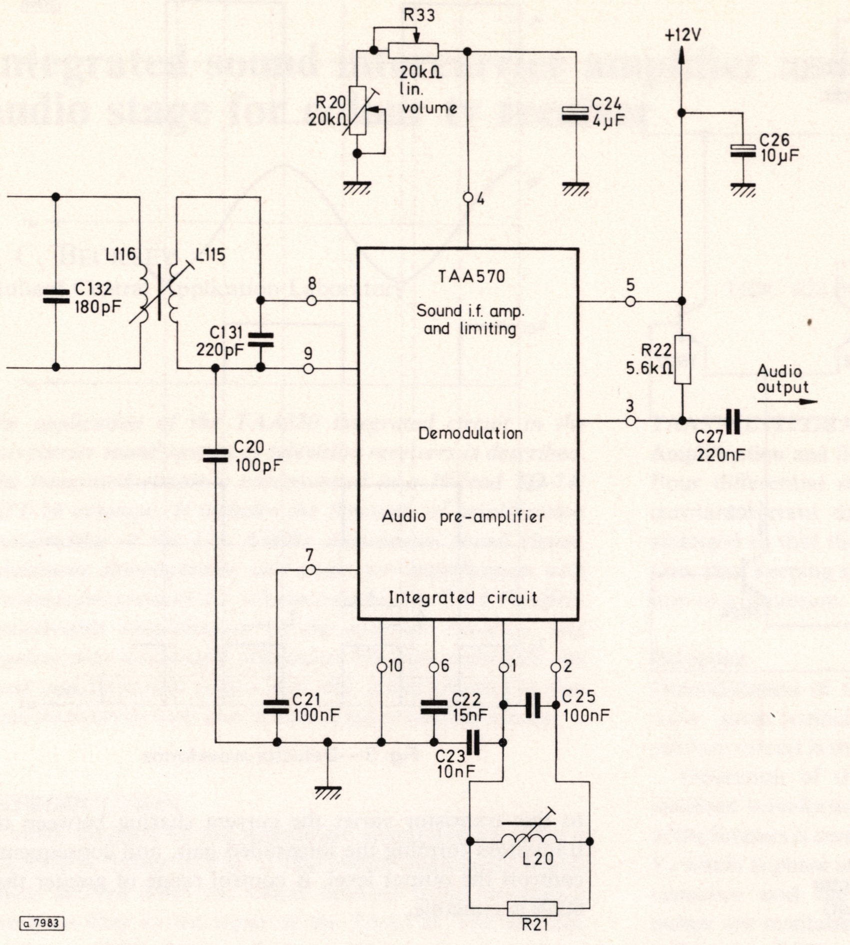
R33
20kΩ
lin.
volume
R20
20kΩ
C24
4μF
+12V
C26
10μF
4
L116
L115
C132
180pF
8
TAA570
Sound i.f. amp.
and limiting
5
C131
220pF
9
R22
5.6kΩ
Audio
output
3
C27
220nF
Demodulation
C20
100pF
Audio pre-amplifier
7
Integrated circuit
10
6
1
2
C21
100nF
C22
15nF
C25
100nF
C23
10nF
L20
R21
a 7983

Fig. 4—External circuit for the TAA570

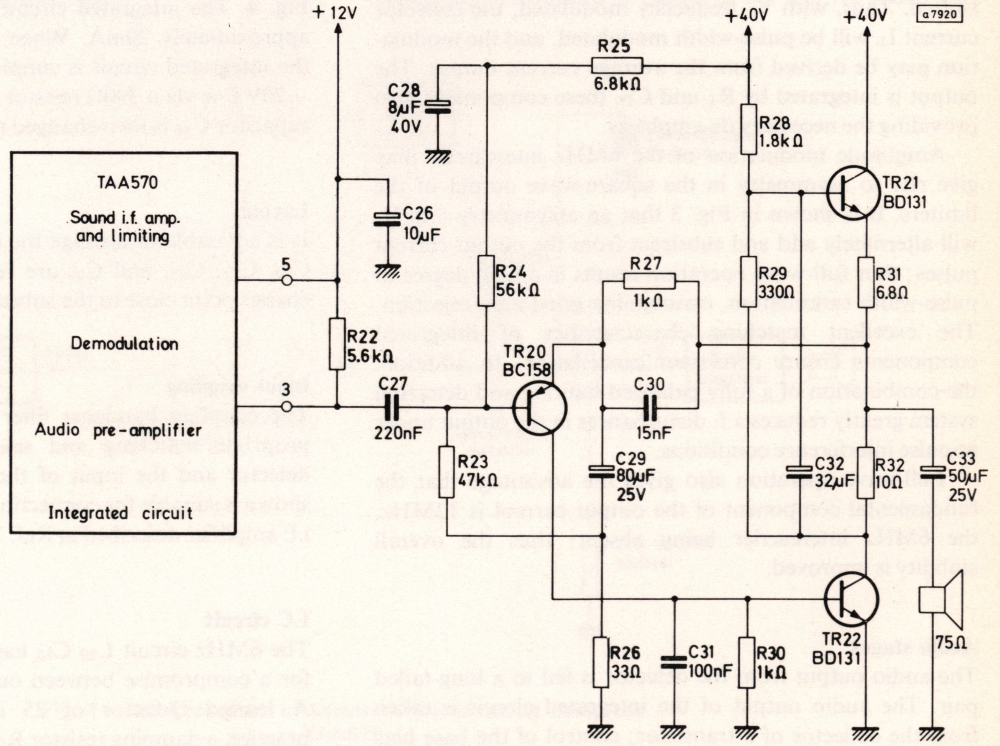
+12V
+40V
+40V
a7920
TAA570
Sound i.f. amp.
and limiting
C28
8μF
40V
R25
6.8kΩ
R28
1.8kΩ
TR21
BD131
C26
10μF
5
R24
56kΩ
R27
1kΩ
R29
330Ω
R31
6.8Ω
Demodulation
R22
5.6kΩ
TR20
BC158
3
C27
220nF
C30
15nF
Audio pre-amplifier
R23
47kΩ
C29
80μF
25V
C32
32μF
R32
10Ω
C33
50μF
25V
Integrated circuit
TR22
BD131
75Ω
R26
33Ω
C31
100nF
R30
1kΩ

Fig. 5—2W audio amplifier

D.C. volume control

The TAA570 gives maximum output with R_{33} at maximum resistance. For this component a 20kΩ linear potentiometer is required; gain control is achieved by linear variation of V_1, which gives a logarithmic variation in output voltage. The preset resistor R_{20} gives adjustment of the minimum power output setting to allow for device spreads.

The d.c. control connection, pin 4, must be decoupled by C_{24} in the receiver to eliminate spurious pick-up of hum, from field and line radiation. However, if the d.c. control facility is not required, C_{24} may be omitted and pin 4 open-circuited.

AUDIO CIRCUIT

The TAA570 provides 600mV of audio at 15kHz deviation, with an output resistance of 5·6kΩ. The audio amplifier should, therefore, have a sensitivity of 500mV for full output with an input resistance greater than 10kΩ. To prevent the circuit affecting the supply voltage, class A operation has been chosen.

The circuit shown in Fig. 5 uses two output transistors operating in class A push-pull. Transistor TR_{22} has a resistor in its collector, the voltage across which is used to drive transistor TR_{21}. Feedback is applied to the emitter of the input transistor, which also serves as a d.c. comparator to fix the mid-point voltage.

PERFORMANCE

Integrated circuit

Supply voltage	12V
Total current drain	approx. 20mA
y parameters at 6MHz	
Input admittance pin 8	250 + j475μmho
Output admittance pin 2	100 + j400μmho
Typical V_o for Δf of 15kHz at 1kHz	600mV r.m.s.
Maximum distortion for Δf of 50kHz at 1kHz	3%

A.M. rejection and limiting characteristics

Typical a.m. rejection and a.f. limiting characteristics are shown in Fig. 6. The input voltage V_{in} when V_o is 3dB below maximum is approximately 100μV. The a.m. rejection is some 25dB at 1mV input, rising to about 40dB at 4mV. A useful level of a.m. rejection is preserved down to very low values of input signal.

Audio output and remote control range

Minimum gain control range	60dB
Power output	2W
Sensitivity	450mV for 2W
Bandwidth (−3dB)	70Hz to 14kHz
Input resistance	30kΩ
Total current	130mA

ALIGNMENT

The detector coil L_{20} is tuned for maximum audio output, with adequate input signal for limiting, making alignment very easy.

The input bandpass filter primary L_{116} and secondary L_{115} may also be tuned for maximum a.f. output if the modulated 6MHz input signal is reduced below that for limiting, that is below 100μV.

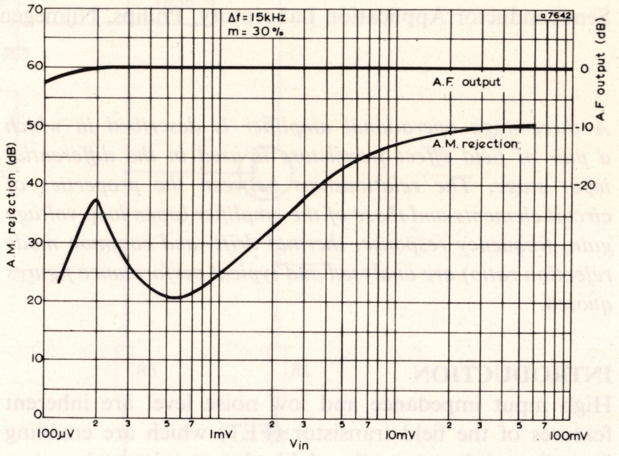

Fig. 6—Typical a.m. rejection and a.f. limiting characteristics

INDUCTORS

Inductor	Former	Core	Wire	Number of turns
L_{115}	P1003/1	4×0·5×6mm grade 900	42 s.w.g. t.n.a.	27
L_{116}		4×0·5×6mm grade 900	42 s.w.g. t.n.a.	30
L_{20}	P1011/1	4×0·5×12·7mm grade 500	42 s.w.g. t.n.a.	40

L_{115} and L_{116} are wound with earthy ends together, spaced by 1mm.

Formers P1003/1 and P1011/1 are $\frac{3}{16} \times 1\frac{1}{2}$ in and $\frac{3}{16} \times \frac{3}{4}$ in respectively with screening cans; they are supplied by E.I.H. Electronics Limited.

HEATSINKS

Each output transistor dissipates 2·4W, and a heatsink of at least 15cm² per device is required, for a maximum ambient temperature of 55°C, with free-air vertical mounting and no mica washers. If mica washers are used, at least 20cm² per device should be used. A thermal jointing compound is recommended.

REFERENCES

1. Bissmire, P., 'Single System I.F. Amplifier for U.K. 625-line System'. **Mullard Technical Communications**, Vol. 10, No. 98, March 1969, pp. 234 to 243.

Matched field effect transistors in the differential input stage of an operational amplifier

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UDC 621.375.132.024[621.317.083.6]:621.382.323

A three-stage operational amplifier is described in which a pair of field effect transistors is used in the differential input stage. The relationships between the properties of circuit elements and those of the amplifier (open loop voltage gain, frequency response, thermal drift, and common mode rejection ratio) are analysed and typical performance figures quoted.

INTRODUCTION

High input impedance and low noise level are inherent features of the field transistor (FET) which are enabling it to supersede conventional bipolar transistors in many applications. The input resistance of the FET is that of a reverse biased diode and is higher than that associated with any configuration of junction transistors. It is limited primarily by the leakage current in the gate circuit, I_{GSS}. The magnitude of I_{GSS} is very small (0·5nA maximum for the BFS21A type FET at room temperature) which results in a minimum input resistance of $10^{10}\Omega$.

The FET is particularly suitable for use in the differential input stage of an operational amplifier. Bias and offset currents can be reduced by a factor of 10^3 compared with those of a similar stage equipped with bipolar transistors. There is no such advantage with regard to offset voltage and thermal drift but these can be kept to the same order of magnitude as with bipolar transistors when matched pairs of FETs are used.

From a practical viewpoint this means that an amplifier equipped with FETs will maintain its overall gain accuracy even with high source impedance. Moreover, the superior noise performance of FETs under conditions of low frequency and high source impedance gives them a decided advantage over bipolar transistors.

It is important to ensure that the voltage gain of the complete amplifier is sufficiently high for operational use. In order to do this, an understanding is desirable of how the properties of the complete amplifier are related to those of circuit elements. To begin with, therefore, some of the properties of an operational amplifier will be examined.

ANALYSIS OF THE PROPERTIES OF THE OPERATIONAL AMPLIFIER

The analysis will be based on the circuit shown in Fig. 1 which is a three-stage difference amplifier with a pair of FETs in the first stage. To maintain voltage levels the bipolar transistors in one of the subsequent stages must be of the p-n-p type. If the second stage is chosen a slight improvement in frequency response is obtained but very close matching of the transistors for h_{FE} is then necessary. If the third stage is chosen, however, this limitation does not apply.

In principle it is possible to use only one transistor instead of two in the third stage. However, an emitter resistor is then needed to adjust the current, and the voltage gain suffers. Likewise, the output signal can be taken directly from the third stage but, for low output impedance, an emitter follower is interposed.

The following circuit properties will be described:

open loop voltage gain,
common mode and supply rejection ratios,
thermal drift,
frequency response.

Open loop voltage gain

In the following analysis the terms transconductance g_{fs} and output conductance g_{os} are used in place of the terms transfer admittance y_{fs} and output admittance y_{os} which are quoted in the published data on FETs. At low frequencies this is reasonable since susceptance terms can be ignored and it may be assumed that admittance is equal to conductance.

Unlike the transconductance of the bipolar transistor, which varies directly as the collector current, that of the FET varies approximately as the square root of the drain current. Thus, for a given second stage load resistance, there is a corresponding drain current I_D at which the loop voltage gain A_1 of the first stage is a maximum. With bipolar transistors there is no such maximum. This is explained as follows.

The differential voltage gain of the first stage is given by:

$$A_1 = -\frac{g_{fs1}R_1R_{i2}}{R_1+R_{i2}}, \qquad \ldots(1)$$

where R_1 is the drain resistance of the first stage, R_{i2} is half the input resistance of the second stage, and g_{fs1} is the transconductance of one of the FETs.

The transconductance g_{fs1} is given by:

$$g_{fs1} = \frac{2}{V_p}(I_D I_{DSS})^{\frac{1}{2}}, \qquad \ldots(2)$$

where V_p is the pinch-off voltage, I_D is the drain current and I_{DSS} is the drain current at zero gate-to-source voltage (Ref. 1).

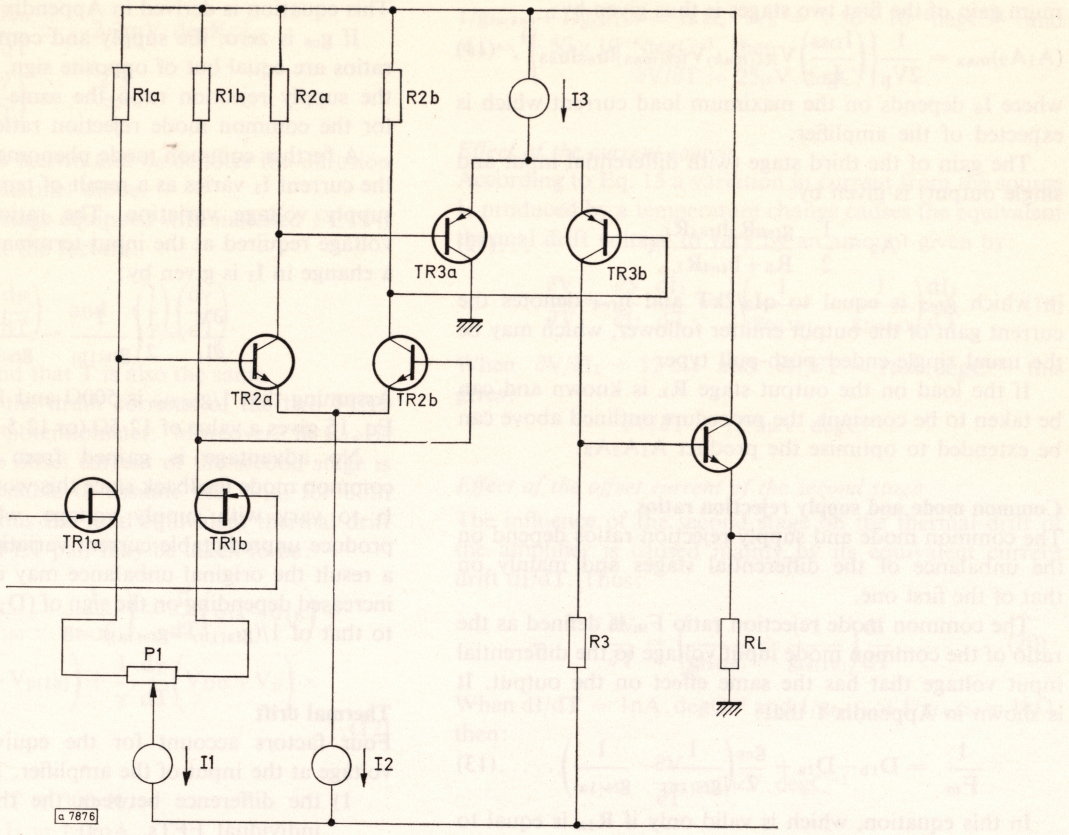

Fig. 1—Simplified circuit of a three-stage difference amplifier with matched FETs at the input

There is a further relationship between the drain current I_D and the drain resistance R_1 which must be observed. The drain-to-gate voltage should preferably not fall below the knee. In no event should it fall so low as to open the gate-channel diode even when the maximum permissible positive common mode voltage is present at the amplifier input. This implies that at a given supply voltage the drop across the drain resistance must not exceed a value which depends, not only on the supply voltage and the maximum common mode voltage being dealt with, but also on the knee characteristic of the FET. By combining Eqs. 1 and 2 and substituting V_{R1}/R_1 for I_D, it can be shown by differentiation that A_1 is a maximum when:

$$R_1 = R_{i2}, \qquad \ldots(3)$$

and

$$I_D = V_{R1(max)}/R_{i2}. \qquad \ldots(4)$$

In other words the maximum gain occurs when the total current to the first stage I_1 is $2V_{R1(max)}/R_{i2}$.

The maximum gain is then:

$$A_{1(max)} = -\left(\frac{1}{V_p}\right)(I_{DSS}V_{R1(max)}R_{i2})^{\frac{1}{2}}. \qquad \ldots(5)$$

The gain of the second stage is given by:

$$A_2 = -\frac{g_{fe2}R_2R_{i3}}{R_2+R_{i3}}, \qquad \ldots(6)$$

in which g_{fe2} is the transconductance of one of the second stage transistors, R_2 is the collector resistance of the same transistor and R_{i3} is half the input resistance of the third stage. The transconductance g_{fe2} is given by:

$$g_{fe2} = \frac{qI_2}{2kT} = \frac{h_{fe2}}{R_{i2}}, \qquad \ldots(7)$$

where I_2 is the total current of the second stage, q is the electronic charge, k is Boltzmann's constant, T is the temperature in degrees Kelvin and h_{fe2} is the forward current transfer ratio.

Again, the voltage drop across R_2 must not exceed a certain maximum. By substituting:

$$I_2 = \frac{2V_{R2}}{R_2} \qquad \ldots(8)$$

in Eq. 7 and combining Eqs. 5 and 6 it can be shown that $A_{1(max)}A_2$ reaches a maximum when:

$$R_2 = R_{i3}, \qquad \ldots(9)$$

and

$$I_2 = \frac{2V_{R2(max)}}{R_{i3}}, \qquad \ldots(10)$$

where $V_{R2(max)}$ depends on $V_{R1(max)}$ and the permissible collector-base voltage of the second stage and:

$$R_{i3} = \frac{2kT\,h_{fe3}}{qI_3}.$$

I_3 denotes the total current of the third stage. The maximum gain of the first two stages is thus given by:

$$(A_1A_2)_{max} = \frac{1}{2V_p}\left\{\left(\frac{I_{DSS}}{I_3}\right)V_{R1(max)}V_{R2(max)}h_{fe2}h_{fe3}\right\}^{\frac{1}{2}}, \quad (11)$$

where I_3 depends on the maximum load current which is expected of the amplifier.

The gain of the third stage (with differential input and single output) is given by:

$$A_3 = \frac{1}{2}\cdot\frac{g_{fe3}R_3h_{fe4}R_L}{R_3+h_{fe4}R_L}, \quad \ldots(12)$$

in which g_{fe3} is equal to $qI_3/2kT$ and h_{fe4} denotes the current gain of the output emitter follower, which may be the usual single-ended push-pull type.

If the load on the output stage R_L is known and can be taken to be constant, the procedure outlined above can be extended to optimise the product $A_1A_2A_3$.

Common mode and supply rejection ratios

The common mode and supply rejection ratios depend on the unbalance of the differential stages and mainly on that of the first one.

The common mode rejection ratio F_m is defined as the ratio of the common mode input voltage to the differential input voltage that has the same effect on the output. It is shown in Appendix 1 that:

$$\frac{1}{F_m} = D_{1b}-D_{1a}+\frac{g_{cs}}{2}\left(\frac{1}{g_{fs(1b)}}-\frac{1}{g_{fs(1a)}}\right). \quad \ldots(13)$$

In this equation, which is valid only if R_{1a} is equal to R_{1b}, D denotes the penetration factor (Durchgriff) of the FET. This is defined as the ratio of the output conductance g_{os} to the transconductance g_{fs} where g_{cs} is the output conductance of the current source I_1 and the subscripts 1_a and 1_b denote the two FETs.

The D-terms in Eq. 13 account for one aspect of the common mode rejection and the g-terms for another. If g_{cs} is zero, the last term vanishes and F_m is determined solely by the penetration factors. Thus, if D_{1a} is 1/100 and D_{1b} is 1/95, for example, F_m is 2×10^3 or 66dB. Similarly if the penetration factors are equal, the first two terms in Eq. 13 cancel and F_m depends solely on the conductances. In this case, if g_{cs} is $1\mu A.V^{-1}$, $g_{fs(1a)}$ is $2{\cdot}0mA.V^{-1}$ and $g_{fs(1b)}$ is $2{\cdot}1mA.V^{-1}$ then F_m is $8{\cdot}4\times10^4$ or 98dB. Thus, in the present instance, the total common mode rejection ratio is determined mainly by the D-terms.

The penetration factors of the FETs are commonly of the order of 10^{-2} to 10^{-3}, and for a matched pair, are generally within ±5% of each other. To obtain a high common mode rejection ratio it is therefore important to choose FETs not only with the highest possible transconductances but also with the smallest possible penetration factors. Also, it is important that the output conductance of the current source g_{cs} should be as low as practicable.

As with common mode voltages, a change in supply voltage can also give rise to spurious output voltages. The supply rejection ratio Fs, defined as the ratio of the change in positive supply voltage to the differential input voltage that has the same effect on the output, is given by:

$$\frac{1}{F_s} = D_{1a}-D_{1b}+\frac{g_{cs}}{2}\left(\frac{g_{os(1a)}-g_{os(1b)}}{g_{fs(1a)}g_{fs(1b)}}\right). \quad \ldots(14)$$

This equation is derived in Appendix 2.

If g_{cs} is zero, the supply and common mode rejection ratios are equal but of opposite sign. In order to improve the supply rejection ratio the same arguments apply as for the common mode rejection ratio.

A further common mode phenomenon is that in which the current I_1 varies as a result of temperature or negative supply voltage variation. The ratio of the differential voltage required at the input terminals to compensate for a change in I_1 is given by:

$$\frac{\partial V}{\partial I_1} = \frac{1}{2}\left(\frac{1}{g_{fs(1b)}}-\frac{1}{g_{fs(1a)}}\right). \quad \ldots(15)$$

Assuming that $1/g_{fs(1b)}$ is 500Ω and $1/g_{fs(1a)}$ is 475Ω then Eq. 15 gives a value of 12·5Ω (or $12{\cdot}5\mu V.\mu A^{-1}$) for $\partial V/\partial I_1$.

No advantage is gained from the application of common mode feedback since this would cause the current I_1 to vary with supply voltage, which in turn would produce unpredictable current variations in the FETs. As a result the original unbalance may either be lessened or increased depending on the sign of $(D_{1a}-D_{1b})$ with respect to that of $1/(g_{fs(1b)}-g_{fs(1a)})$.

Thermal drift

Four factors account for the equivalent thermal drift voltage at the input of the amplifier. These are:

1) the difference between the thermal drifts of the individual FETs,
2) the difference between the temperature coefficients of the drain resistors R_{1a} and R_{1b},
3) thermal drift of the current source,
4) thermal drift of the offset current of the second stage.

In theory, the thermal drift of the offset voltage of the second stage is also a factor, but in practice it can be disregarded. Each of the four factors above will be examined separately, taking the others to be absent in each case.

Effect of the FETs

For a single FET the equivalent thermal drift voltage is given by:

$$\left(\frac{dV_{gs}}{dT}\right)_{I_D} = \frac{1}{\mu}.\frac{d\mu}{dT}.\frac{I_D}{g_{fs}}-\frac{dV_p}{dT}+\frac{D}{\gamma}.\frac{d\gamma}{dT}(V_{DG}+V_p) \quad \ldots(16)$$

where μ is the mobility of the majority carriers in the channel, V_p is the pinch-off voltage, V_{DG} is the drain-gate voltage and

$$\gamma = \frac{\mu V_p}{Lu_{max}}$$

in which L is the channel length (from drain to source) and u_{max} is the saturation velocity of majority carriers in silicon.

The following approximations can be made:

$$\left(\frac{1}{\mu}\right)\left(\frac{d\mu}{dT}\right) \simeq -\frac{1{\cdot}5}{T},$$

$$\frac{dV_p}{dT} = \frac{d\phi_o}{dT} \simeq -2{\cdot}2mV.degK^{-1},$$

$$\left(\frac{1}{\gamma}\right)\left(\frac{d\gamma}{dT}\right) \simeq -\frac{2{\cdot}3}{T},$$

where T is in degrees Kelvin and ϕ_0 denotes the diffusion voltage of the gate-channel diode.

For a differential stage equipped with matched FETs it may be assumed that the factors:

$$\left(\frac{1}{\mu}\right)\left(\frac{d\mu}{dT}\right) \text{ and } \left(\frac{1}{\gamma}\right)\left(\frac{d\gamma}{dT}\right)$$

are equal for both, and that T is also the same.

In the first stage the drain currents of the two FETs are equalised by a potentiometer. Moreover, if R_{1a} is equal to R_{1b} and the offset current of the second stage is negligible, it is reasonable to assume that V_{DG} for both FETs is the same. Thus the total equivalent thermal drift input voltage of the FET pair may be taken to be:

$$\frac{\partial V}{\partial T} = \frac{I_1}{2\mu}.\frac{d\mu}{dT}\left(\frac{1}{g_{fs(1a)}}-\frac{1}{g_{fs(1b)}}\right)-\frac{d}{dT}\left(\phi_{1a}-\phi_{1b}\right)+$$
$$+\frac{D_1}{\gamma}.\frac{d\gamma}{dT}\left(V_{p(1a)}-V_{p(1b)}\right)+\frac{1}{\gamma}.\frac{d\gamma}{dT}\left(V_{DG}+V_p\right)\times$$
$$\times(D_{1a}-D_{1b}). \quad \ldots(17)$$

If it is assumed that:

$$T = 300\text{ K},$$
$$I_1 = 1{\cdot}0mA,$$
$$g_{fs(1a)} = 2{\cdot}1mA.V^{-1},$$
$$g_{fs(1b)} = 2{\cdot}0mA.V^{-1},$$
$$V_p = (V_{p(1a)}-V_{p(1b)})/2,$$
$$V_{p(1a)}-V_{p(1b)} = 20mV,$$
$$D = (D_{1a}+D_{1b})/2 = 10^{-2},$$
$$D_{1a}-D_{1b} = 5\times10^{-4},$$
$$\phi_{1a}-\phi_{1b} = 3mV,$$
$$V_{DG}+V_p = 10V,$$

then the separate components of drift in Eq. 17 are:

$$\frac{I_1}{2\mu}.\frac{d\mu}{dT}\left(\frac{1}{g_{fs(1a)}}-\frac{1}{g_{fs(1b)}}\right) = 60\mu V.degC^{-1},$$

$$\frac{d}{dT}(\phi_{1a}-\phi_{1b}) = \frac{\phi_{1a}-\phi_{1b}}{T} \simeq 10\mu V.degC^{-1},$$

$$\frac{D_1}{\gamma}.\frac{d\gamma}{dT}(V_{p(1a)}-V_{p(1b)}) = -1{\cdot}5\mu V.degC^{-1},$$

$$\frac{1}{\gamma}.\frac{d\gamma}{dT}(V_{DG}+V_p)(D_{1a}-D_{1b}) \simeq -40\mu V.degC^{-1}.$$

The first and fourth of these components easily outweigh the others which explains why FETs well matched for transconductance and output resistance are required in this application.

Effect of the drain resistance

The extent to which the inequality of the two drain resistances contributes to the equivalent thermal drift is given by:

$$\frac{\partial V}{\partial T} = (\alpha_{1b}-\alpha_{1a}).\frac{I_1}{2}\left(\frac{1}{g_{fs(1a)}}+\frac{1}{g_{fs(1b)}}\right), \quad \ldots(18)$$

where $\alpha = (1/R).(dR/dT)$. If it is assumed that $I_1 = 1mA$, $1/g_{fs(1a)}+1/g_{fs(1b)} = 1k\Omega$, $\alpha_{1b} = +50\times10^{-6}degC^{-1}$ and $\alpha_{1a} = -50\times10^{-6}degC^{-1}$, then

$$\partial V/\partial T = 25\mu V.degC^{-1}.$$

Effect of the current source

According to Eq. 15 a variation in current from the source I_1 produced by a temperature change causes the equivalent thermal drift voltage to vary by an amount given by:

$$\frac{\partial V}{\partial T} = \frac{\partial V}{\partial I_1}.\frac{dI_1}{dT} = \frac{1}{2}\left(\frac{1}{g_{fs(1b)}}-\frac{1}{g_{fs(1a)}}\right)\frac{dI_1}{dT}. \quad \ldots(19)$$

When $\partial V/\partial I_1 = 12{\cdot}5\Omega$ and $\partial I_1/\partial T = 1\mu A.degC^{-1}$ this gives:

$$\partial V/\partial T = 12{\cdot}5\mu V.degC^{-1}.$$

Effect of the offset current of the second stage

The influence of the second stage on the thermal drift of the amplifier is caused mainly by its equivalent current drift dI/dT. Thus:

$$\frac{\partial V}{\partial T} = \left(\frac{1}{g_{fs(1a)}}+\frac{1}{g_{fs(1b)}}\right)\frac{dI}{dT}. \quad \ldots(20)$$

When $dI/dT = 1nA.degC^{-1}$ and $1/g_{fs(1a)}+1/g_{fs(1b)} = 1k\Omega$, then:

$$\frac{\partial V}{\partial T} = 1\mu V.degC^{-1}.$$

Poles in the complex plane

Without frequency compensation

Because of the collector capacitances, the wiring capacitances, and transistor cut-off frequencies, the voltage gain of the amplifier decreases with frequency. The frequency response is determined by three poles in the complex plane. Close to unity gain, the roll-off (the rate at which the gain decreases with frequency) is 12dB to 18dB per octave, which means that without compensation the amplifier may be unstable when external feedback is applied.

The first and third poles are determined by the third stage. Thus:

$$p_1 = \frac{-\omega_{(hfb)3}\left(\frac{1}{h_{fe3}}+\frac{1}{R_2g_{fe3}}\right)}{1+\omega_{(hfb)3}C_{f3}R_3'}, \quad \ldots(21)$$

at a frequency f_1 of about 30kHz, and

$$p_3 = -\frac{1+\omega_{(hfb)3}C_{f3}R_3'}{R_3'(C_{f3}+C_{o3}+C_3')}, \quad \ldots(22)$$

at a frequency f_3 of about 20MHz.

Equations 21 and 22 are derived in Appendix 3.

In these expressions C_{f3} is the collector-to-base capacitance, C_{o3} the collector-to-emitter capacitance, and C_3' the total load capacitance of the transistor in the third stage. R_3' denotes the total load resistance of the third stage which is given by:

$$R_3' = R_3/h_{fe4}R_L.$$

$\omega_{(hfb)3}$ is the angular cut-off frequency at which h_{fb} has dropped by 3dB.

The second pole is determined by the angular cut-off frequency $\omega_{(hfb)2}$ of the second stage. Thus:

$$p_2 = -\,\omega_{(hfb)2}\left(\frac{1}{h_{fe2}} + \frac{1}{g_{fe2}R_1}\right), \qquad \ldots(23)$$

at a frequency f_2 of about 1MHz.

Equation 23 is derived in Appendix 3.

The influence of the emitter follower stage can be disregarded as its poles lie outside the frequency range of interest.

With frequency compensation

To ensure that the amplifier will be stable with any combination of feedback and load, the transfer function F_p/G_p should be characterised by no more than one pole up to, and preferably beyond, the frequency at which the gain has fallen to unity.

A frequency compensating network consisting for example of a resistor and a capacitor in series, or merely of a capacitor, can be incorporated to satisfy this condition. In the circuit to be described an RC network is connected between the bases of the second-stage transistors. This not only introduces an additional pole p_o but also a zero z_1 equal to 1/RC. To make zero z_1 compensate for pole p_1, R and C should be chosen so that the following condition is satisfied:

$$1/RC = z_1 = p_1. \qquad \ldots(24)$$

The pole p_o then becomes:

$$p_o = \frac{R_1 + R_{i1}}{2CR_1R_{i1}}, \qquad \ldots(25)$$

at a frequency f_o close to 100Hz. (See Fig. 2.)

Since the compensating network is shunted across the input of the second stage, the pole p_2 is shifted far to the left along the real axis to a new position p_2' given by

$$p_2' = \frac{-2\omega_{(hfb)2}}{Rg_{fe2}}. \qquad \ldots(26)$$

In general p_2' lies far below the frequency range of interest because $Rg_{fe2} \ll 1$ and $\omega_{(hfb)2} \simeq 2\pi(100\text{MHz})$.

Equations 25 and 26 are derived in Appendix 3.

The third pole p_3 is unchanged and may give rise to noticeable phase shift at frequencies close to unity gain.

For dimensioning the RC network the unity gain bandwidth f_T of the compensated amplifier is found. This will be smaller than, but the same order of magnitude as, the unity gain bandwidth of the uncompensated amplifier. Above the unity gain point, the gain can be taken to increase by 6dB per octave as frequency decreases and on this basis $f_o = f_T/A_o$ can be found. The required values of R and C can be found from Eqs. 24 and 25.

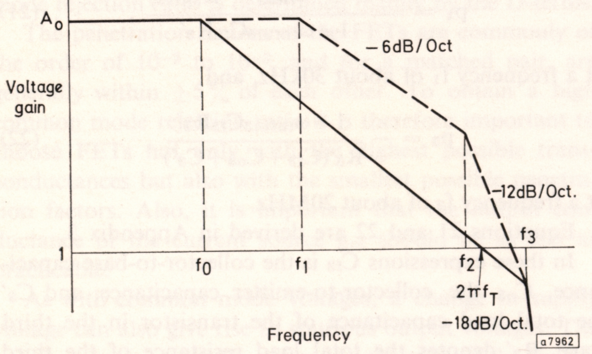

Fig. 2—Frequency response diagram illustrating the effect of the compensation network. The solid line indicates the calculated frequency response with compensation and the broken line that without compensation

Slewing rate

The slewing rate r_s is a measure of the speed with which the output of the amplifier can change from one fully driven condition to the other (Fig. 3) and is expressed by the differential quotient $\Delta V_o/\Delta t$. With a capacitive load the slewing rate is smaller than with a resistive one.

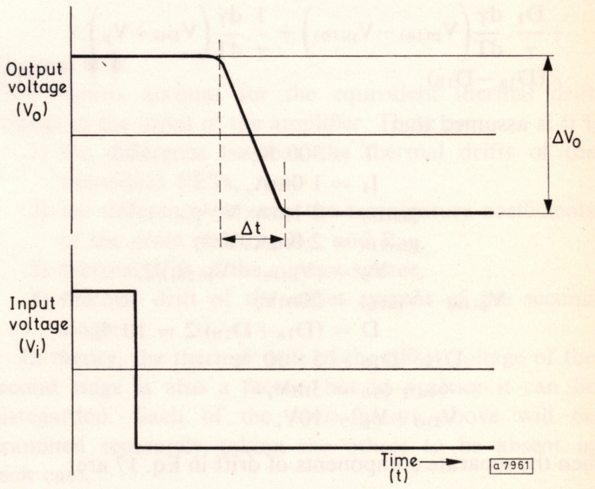

Fig. 3—Input and output voltages plotted against time illustrating the definition of slewing rate

The slewing rate measured without the compensating network varies directly as the d.c. collector current and inversely as the total collector capacitance (plus the load capacitance) of the third stage transistors. As a rule incorporation of a compensating network reduces the slewing rate, particularly if the network is close to the output. On the other hand, the closer the network is to the input the greater will be its effect on the noise properties of the amplifier (for frequencies in excess of f_o).

A high value of compensating network impedance $R + 1/j\omega C$ favours both the slewing rate and the noise properties of the amplifier. However, the optimum values of R and C are dictated by Eqs. 24 and 25. The situation can be improved by raising the cut-off frequency f_T of the amplifier and reducing the gain A_o. This is done by connecting a resistor valued at a few tens of ohms in series with the emitter contacts of the second or third stages, or both. In this way the frequency f_o is also raised so that C can be given a smaller value. This solution is all the more effective because the pole p_1 is shifted to a higher frequency thus diminishing the required value of the time constant, RC.

CIRCUIT DESCRIPTION

Fig. 4 shows the circuit of the complete amplifier having four stages, the first of which uses a matched pair of FETs, type BFS21A. A potentiometer across the source terminals allows the offset voltage to be adjusted to zero. The current I_1 of the first stage is supplied from an amplifier operating with complete feedback which constitutes a source having a very low temperature coefficient and a very small parallel admittance. To prevent variations in current caused by supply voltage fluctuations, the current source is fed by a voltage regulator (zener) diode with a low temperature coefficient.

The common mode and supply rejection ratios and the equivalent voltage drift of the amplifier depend almost exclusively on differences between the FETs (see Eqs. 13 and 14).

To improve the bandwidth and slewing rate, resistors are included in the emitter circuits of the second stage (see section headed *Slewing rate*). At the expense of only a 4dB drop in gain the slewing rate is improved by a factor of four and the unity gain bandwidth is doubled.

The currents I_2 and I_3 in the second and third stages can be safely taken from single resistors without noticeably affecting the common mode and supply rejection ratios or the drift.

No stringent matching is necessary for the p-n-p transistors used in the third stage. The total current supplied by this stage must be sufficient to achieve the required current and voltage drive of the subsequent emitter follower stage.

The emitter follower is a single-ended push-pull type which has a low quiescent current and can be symmetrically driven. To eliminate the flat spot that may occur in the take-over characteristic of such a circuit some emitter current should flow in both transistors even at zero output voltage. This may be provided for by connecting each emitter to the opposite rail via a resistor, as shown by the broken lines in the diagram.

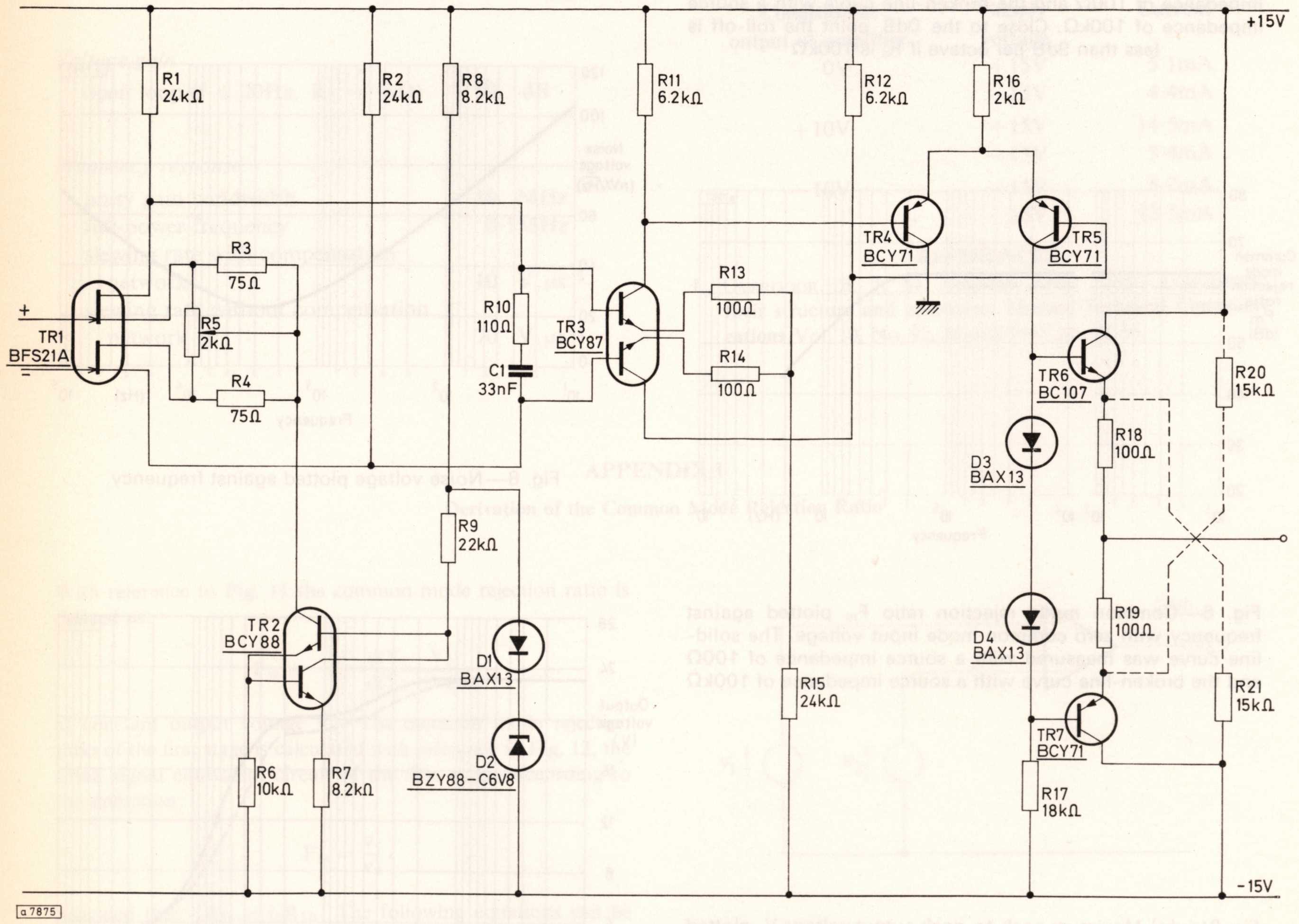

Fig. 4—Circuit of the complete amplifier (R_1 and R_2 are ±0·1% metal film resistors and R_{11} and R_{12} are ±1% resistors. All others have tolerances of ±5%)

Measured results

Measurements of the frequency response, common mode rejection ratio, noise figure, and peak-to-peak voltage of the amplifier are plotted in Figs. 5 to 10.

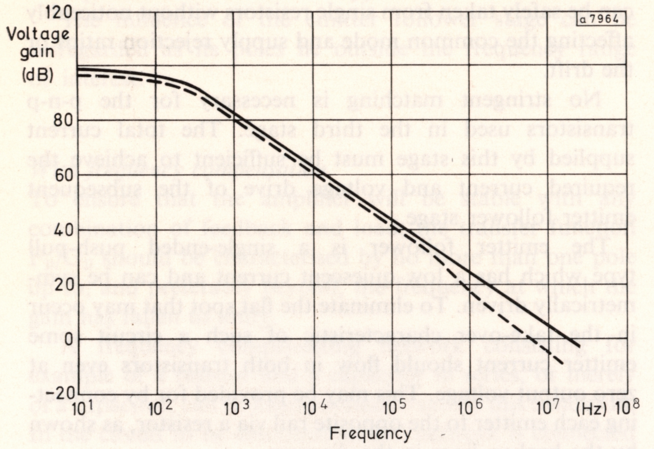

Fig. 5—Frequency response with zero common mode input voltage. The solid-line curve was measured with a source impedance of 100Ω and the broken-line curve with a source impedance of 100kΩ. Close to the 0dB point the roll-off is less than 9dB per octave if R_s is 100kΩ

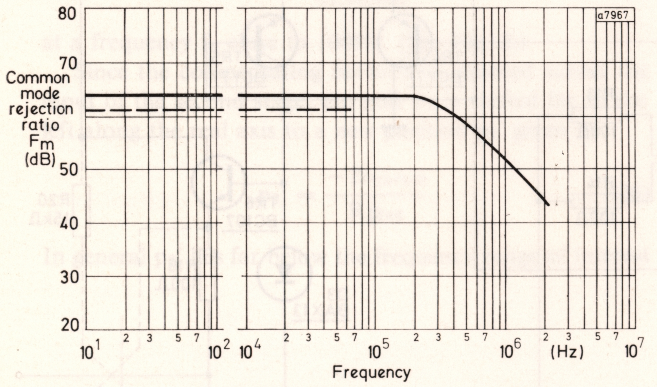

Fig. 6—Common mode rejection ratio F_m plotted against frequency with zero common mode input voltage. The solid-line curve was measured with a source impedance of 100Ω and the broken-line curve with a source impedance of 100kΩ

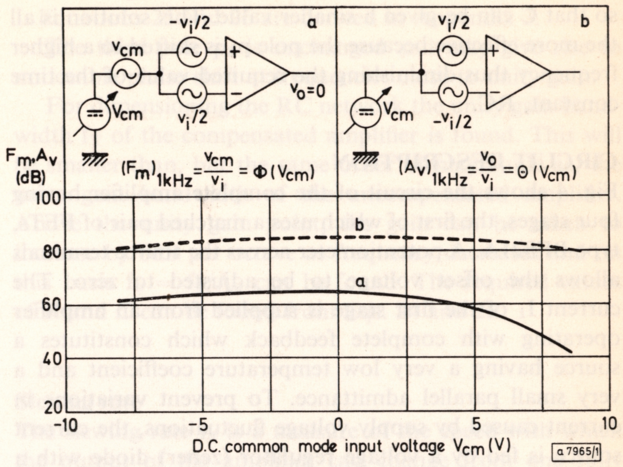

Fig. 7—Common mode rejection ratio v_{cm}/v_i (solid line) as defined by circuit a and voltage gain v_o/v_i (broken line) as defined by circuit b plotted against d.c. common mode input voltage, V_{cm}. For both measurements the frequency of v_{cm} and v_i was 1kHz

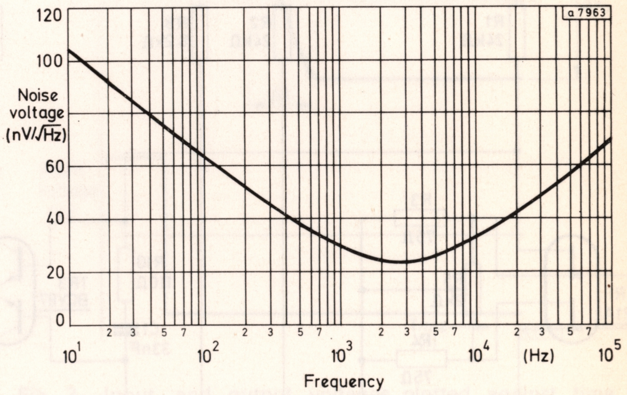

Fig. 8—Noise voltage plotted against frequency

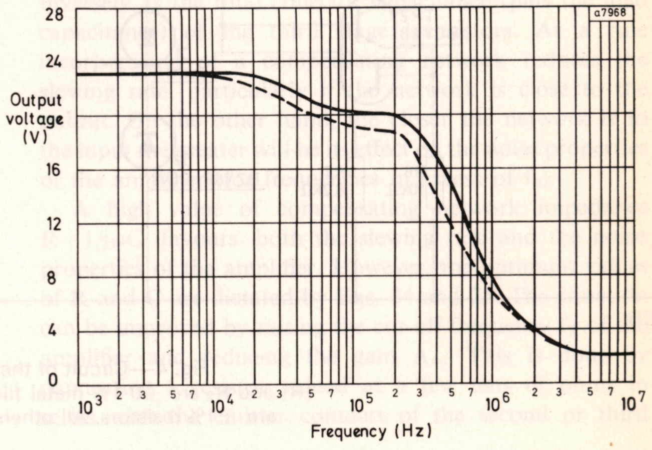

Fig. 9(right) Maximum peak-to-peak output voltage V_o plotted against frequency at a total distortion of 10%. Measurements for the solid-line curve were made with a load resistance of 100kΩ and those for the broken-line curve with a load resistance of 1kΩ

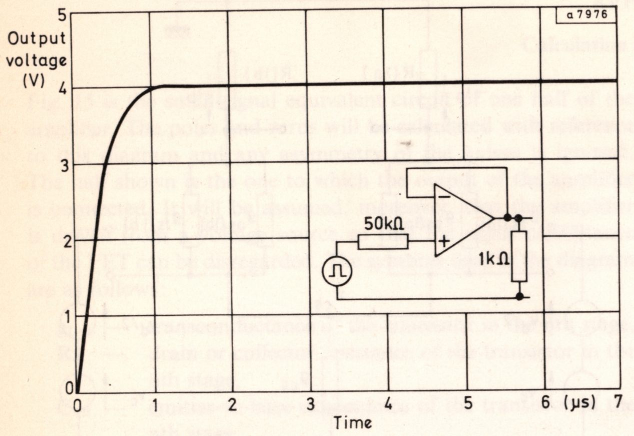

Fig. 10—Response to an input voltage step

Representative performance figures measured at supply voltages of +15V and −15V (and at an ambient temperature of 25°C unless otherwise stated) are tabulated below.

Voltage gain

open loop (f ⩽ 20Hz, R_L = 1kΩ)	99	dB

Frequency response

unity gain bandwidth	10	MHz
full-power frequency	0·1	MHz
slewing rate with compensation network	10	V.µs⁻¹
slewing rate without compensation network	70	V.µs⁻¹

Input current

bias current at 25°C	100	pA
bias current at 85°C	5	nA
offset current at 25°C	10	pA
offset current at 85°C	500	pA

Input impedance

differential mode	10 10	GΩ pF
common mode	10 2	GΩ pF

Output

resistance	400	Ω

Input offset voltage

offset plotted against temperature (0 to 85°C)	40	µV.degC⁻¹
offset plotted against time	40	µV.day⁻¹
noise voltage (bandwidth 100kHz)	20	μV_{rms}
common mode rejection ratio	65	dB
positive supply rejection ratio	500	µV.V⁻¹
negative supply rejection ratio	15	µV.V⁻¹

The supply current requirements with a load of 1kΩ are as follows:

Condition at output of amplifier	Supply voltage	Current
0V	+15V	5·1mA
	−15V	4·4mA
+10V	+15V	14·5mA
	−15V	5·4mA
−10V	+15V	5·7mA
	−15V	13·5mA

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1. Overgoor, B. J. M. Junction Field Effect Transistors: their structure and operation. **Mullard Technical Communications** Vol. 10, No. 92, March 1968 pp. 52-56.

APPENDIX I

Derivation of the Common Mode Rejection Ratio

With reference to Fig. 11 the common mode rejection ratio is defined as:

$$F_m = -\frac{1}{2}\cdot\frac{d(V_1+V_2)}{d(V_1-V_2)},$$

at constant output voltage V_o. The common mode rejection ratio of the first stage is calculated with reference to Fig. 12, the small signal equivalent circuit of the first stage. According to the definition:

$$F_m = \frac{v_c}{v_d},$$

provided that $i_aR_{1a} = i_bR_{1b}$. The following equations can be derived from Fig. 12:

$$(v_c - \tfrac{1}{2}v_d - v_{cs})g_{fs(1a)} - (i_aR_{1a} + v_{cs})g_{os(1a)} = i_a\,,$$

and:

$$(v_c + \tfrac{1}{2}v_d - v_{cs})g_{fs(1b)} - (i_bR_{1b} + v_{cs})g_{os(1b)} = i_b\,.$$

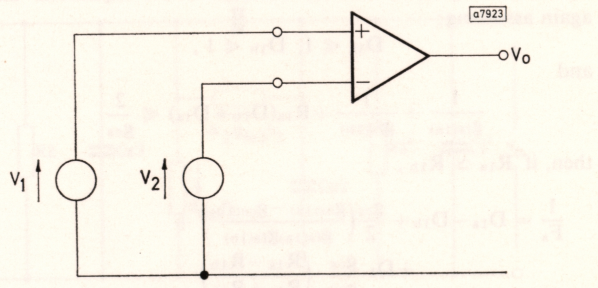

Fig. 11—Voltages considered when defining common mode rejection ratio

Moreover:

$$i_a+i_b = v_{cs}g_{cs}\,,$$

and

$$i_aR_{1a} = i_bR_{1b}\,.$$

By eliminating i_a, i_b and v_{cs} from the equations above and assuming:

$$D_{1a} \ll 1,\ D_{1b} \ll 1,$$

and

$$\frac{1}{g_{fs(1a)}}+\frac{1}{g_{fs(1b)}}+R_{1a}(D_{1b}+D_{1a}) \ll \frac{2}{g_{cs}}\,,$$

then

$$\frac{1}{F_m} = (D_{1b}-D_{1a})\left(1+g_{cs}.\frac{R_{1a}R_{1b}}{R_{1a}+R_{1b}}\right)+ +\frac{g_{cs}}{2}\left(\frac{1}{g_{fs(1b)}}-\frac{1}{g_{fs(1a)}}\right)+\frac{g_{cs}}{g_{fs1}}\left(\frac{R_{1a}-R_{1b}}{R_{1a}+R_{1b}}\right).$$

In this equation g_{fs1} is the average value of $g_{fs(1a)}$ and $g_{fs(1b)}$.

Since $g_{cs}\left(\frac{R_{1a}.R_{1b}}{R_{1a}+R_{1b}}\right) \ll 1$ and $R_{1a} \simeq R_{1b}$

this expression reduces to:

$$\frac{1}{F_m} = D_{1b}-D_{1a}+\tfrac{1}{2}g_{cs}\left(\frac{1}{g_{fs(1b)}}-\frac{1}{g_{fs(1a)}}\right). \qquad \ldots(13)$$

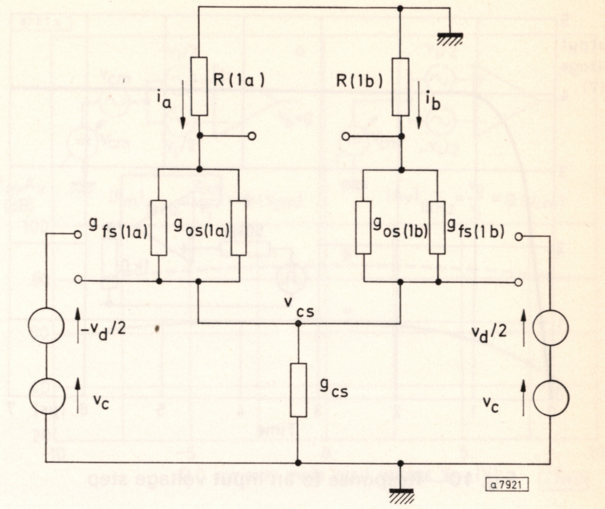

Fig. 12—Small-signal equivalent circuit of the FET-equipped first stage

APPENDIX 2

Derivation of the Supply Mode Rejection Ratio

With reference to Fig. 13 the supply rejection ratio is defined as

$$F_s = -\frac{dV_s}{dV_d}\,,$$

at constant output voltage V_o. The supply rejection ratio of the first stage can be derived with reference to Fig. 14. According to the above definition:

$$F_s = v_s/v_d\,,$$

provided that i_aR_{1a} is equal to i_bR_{1b}.
From the circuit shown in Fig. 14:

$$(-\tfrac{1}{2}v_d-v_{cs})g_{fs(1a)}+(v_s-i_aR_{1a}-v_{cs})g_{os(1a)} = i_a\,,$$

and

$$(\tfrac{1}{2}v_d-v_{cs})g_{fs(1b)}+(v_s-i_bR_{1b}-v_{cs})g_{os(1b)} = i_b\,.$$

Moreover:

$$i_a+i_b = v_{cs}g_{cs}\,,$$

and

$$i_aR_{1a} = i_bR_{1b}\,.$$

By eliminating i_a, i_b and v_{cs} from the above equations and again assuming:

$$D_{1a} \ll 1,\ D_{1b} \ll 1\,,$$

and

$$\frac{1}{g_{fs(1a)}}+\frac{1}{g_{fs(1b)}}+R_{1a}(D_{1b}+D_{1a}) \ll \frac{2}{g_{cs}}\,.$$

then, if $R_{1a} \simeq R_{1b}$,

$$\frac{1}{F_s} = D_{1a}-D_{1b}+\frac{g_{cs}}{2}\left(\frac{g_{os(1a)}-g_{os(1b)}}{g_{fs(1a)}g_{fs(1b)}}\right)+ +D_1.\frac{g_{cs}}{g_{fs1}}.\left(\frac{R_{1a}-R_{1b}}{R_{1a}+R_{1b}}\right).$$

In this equation D_1 is the average value of D_{1a} and D_{1b}.
This reduces to:

$$\frac{1}{F_s} = D_{1a}-D_{1b}+\frac{g_{cs}}{2}\left(\frac{g_{os(1a)}-g_{os(1b)}}{g_{fs(1a)}g_{fs(1b)}}\right)$$

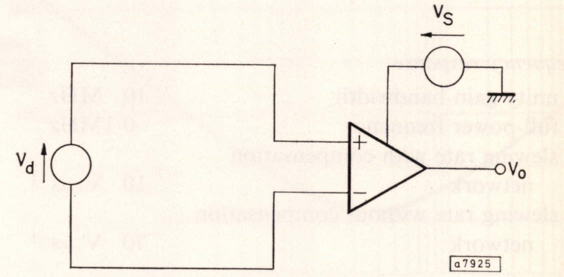

Fig. 13—Voltages considered when defining the supply rejection ratio

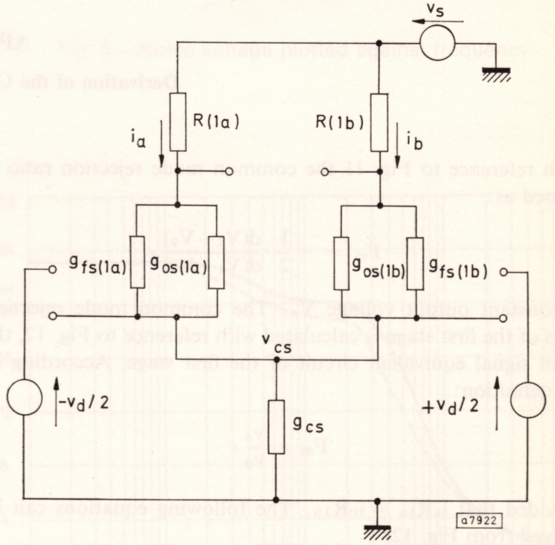

Fig. 14—Small-signal equivalent circuit of the first stage considered when calculating the supply rejection ratio

APPENDIX 3

Calculation of Poles and Zeros

Fig. 15 is the small-signal equivalent circuit of one half of the amplifier. The poles and zeros will be calculated with reference to this diagram and any asymmetry of the halves is ignored. The half shown is the one to which the output of the amplifier is connected. It will be assumed, moreover, that the amplifier is driven from a voltage source so that the input capacitance of the FET can be disregarded. The symbols used in the diagram are as follows:

g_{fen} — transconductance of the transistor in the nth stage,
R_n — drain or collector resistance of the transistor in the nth stage,
C_{en} — emitter-to-base capacitance of the transistor in the nth stage,
C_{on} — emitter-to-collector capacitance of the transistor in the nth stage,
C_{fn} — collector-to-base capacitance of the transistor in the nth stage,
α_n — current gain h_{fbn} of the transistor in the nth stage,
R_3' — total load resistance of the third stage (R_3 in parallel with $h_{fe4}R_4$),
C_3' — total load capacitance of the third stage.

The parasitic series resistances in the emitter, collector, and base leads have no significant effect on the location of poles and zeros and so they may be disregarded.
It is assumed that:

$$y_2 = (1/R_1)+g_{fe2}+p(C_{o1}+C_{e2})+(2pC/1+pRC)\,,$$
$$y_3 = (1/R_2)+g_{fe3}+p(C_{o2}+C_{e3})\,,$$
$$y_4 = (1/R_3')+p(C_{o3}+C_3') = g_4+pC_4\,.$$

Thus:

$$\tfrac{1}{2}v_1g_{fs1}+(y_2-\alpha_2g_{fe2})v_2+(v_2-v_3)pC_{f2} = 0,$$

$$\alpha_2g_{fe2}v_2+(v_3-v_2)pC_{f2}+v_3(y_3-\alpha_3g_{fe3})+(v_3-v_o)pC_{f3} = 0,$$

$$\alpha_3g_{fe3}v_3+(v_o-v_3)pC_{f3}+v_oy_4 = 0.$$

Eliminating v_2 and v_3:

$$\frac{v_o}{v_1} = -\frac{1}{2}\frac{g_{fs1}(\alpha_2g_{fe2}-pC_{f2})(\alpha_3g_{fe3}-pC_{f3})}{y_2A-(\alpha_2g_{fe2}-pC_{f2})B}\,,$$

in which:

$$A = y_4(pC_{f2}+pC_{f3}+y_3-\alpha_3g_{fe3})+pC_{f3}(y_3+pC_{f2})\,,$$

and

$$B = y_4(pC_{f3}+y_3-\alpha_3g_{fe3})+pC_{f3}y_3\,.$$

The factors A and B are identical apart from the term pC_{f2}. As C_{e3} is much larger than C_{f2}, pC_{f2} can be ignored compared with y_3 and A can be considered as approximately equal to B. Therefore:

$$\frac{v_o}{v_2} = -\frac{1}{2}.\frac{g_{fs1}(\alpha_2g_{fe2}-pC_{f2})(\alpha_3g_{fe3}-pC_{f3})}{(y_2-\alpha_2g_{fe2}+pC_{f2})B}\,,$$

$$= -\frac{1}{2}.\frac{g_{fs1}(\alpha_2g_{fe2}-pC_{f2})(\alpha_3g_{fe3}-pC_{f3})}{(y_2-\alpha_2g_{fe2}+pC_{f2})\{y_4(pC_{f3}+y_3-\alpha_3g_{fe3})+pC_{f3}y_3\}}.$$

If there is no compensation network present, then:

$$z_2 = \alpha_2g_{fe2}/C_{f2} \text{ and } z_3 = \alpha_3g_{fe3}/C_{f3}.$$

Both z_2 and z_3 are close to 1GHz and lie outside the frequency range of interest.

Two poles are found from the second term in the denominator.
Thus:

$$\begin{aligned} y_4(pC_{f3}+y_3-\alpha_3g_{fe3})+pC_{f3}y_3 &= p^2\{C_4(C_{f3}+C_{o2}+C_{e3})+C_{f3}(C_{o2}+C_{e3})\}+ \\ &\quad +p\{C_4(1-\alpha_3)g_{fe3}+(C_4/R_2)+g_4(C_{f3}+C_{e3}+C_{o2})+ \\ &\quad +C_{f3}(g_{fe3}+[1/R_2])\}+g_4\{(1-\alpha_3)g_{fe3}+(1/R_2)\}. \end{aligned}$$

In a quadratic equation of the type ap^2+bp+c in which b^2 is much larger than 4ac, the roots are equal to $-b/a$ and $-c/b$. Applying this to the above equation:

$$p_1 = \frac{-[g_4\{(1-\alpha_3)g_{fe3}+(1/R_2)\}]}{C_4(1-\alpha_3)g_{fe3}+(C_4/R_2)+g_4(C_{f3}+C_{e3}+C_{o2})+(g_{fe3}+[1/R_2])C_{f3}}\,,$$

and:

$$p_3 = -\frac{C_4(1-\alpha_3)g_{fe3}+(C_4/R_2)+g_4(C_{f3}+C_{e3}+C_{o2})+(g_{fe3}+[1/R_2])C_{f3}}{C_4(C_{f3}+C_{o2}+C_{e3})+C_{f3}(C_{o2}+C_{e3})}$$

Since:

$$g_4C_{e3}+g_{fe3}C_{f3} \gg C_4(1-\alpha_3)g_{fe3}+(C_4/R_2)+ +g_4(C_{f3}+C_{o2})+(C_{f3}/R_2)\,,$$

and

$$C_{e3} \gg C_{f3}+C_{o2}\,,$$

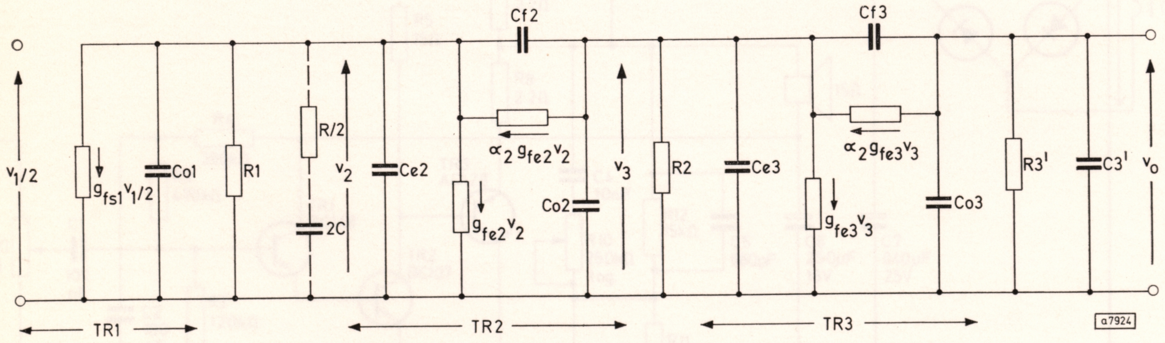

Fig. 15—Small-signal equivalent circuit of one half of the amplifier considered when calculating the poles and zeros determining the frequency response

then, putting $g_{fe3}/C_{e3} = \omega_{(hfb)3}$, these expressions reduce to:

$$p_1 = -\omega_{(hfb)3}\cdot\frac{\left(\frac{1}{h_{fe3}}+\frac{1}{R_2 g_{fe3}}\right)}{1+\omega_{(hfb)3}C_{f3}R_3'} \qquad \ldots(21)$$

and

$$p_3 = -\frac{1+\omega_{(hfb)3}C_{f3}R_3'}{R_3'(C_{f3}+C_{o3}+C_3')} \qquad \ldots(22)$$

where $\omega_{(hfb)3}$ is the cut-off frequency of the transistor in the third stage (the frequency at which h_{fb} has dropped by 3dB).

The pole p_2 is found by putting:

$$y_2-\alpha_3 g_{fe2}+pC_{f2} = 0.$$

If the compensating network (C = 0) is disregarded, this gives:

$$g_{fe2}(1-\alpha_2)+(1/R_1)+p(C_{e2}+C_{o1}+C_{f2}) = 0,$$

or, since $C_{e2} \gg C_{o1}+C_{f2}$:

$$p_2 = -\frac{g_{fe2}}{C_{e2}}\left(\frac{1}{\alpha_2'}+\frac{1}{g_{fe2}R_1}\right) = \omega_{(hfb)2}\left(\frac{1}{h_{fe2}}+\frac{1}{g_{fe2}R_1}\right). \qquad \ldots(23)$$

A compensation network gives rise to an additional zero point and the pole p_2 is replaced by two other poles:

$$\frac{1}{y_2-\alpha_2 g_{fe2}+pC_{f2}} = $$

$$\frac{1+pCR}{\{(1-\alpha_2)g_{fe2}+(1/R_1)+p(C_{e2}+C_{f2}+C_{o1})\}(1+pRC)-2pC}.$$

The new zero point $z_1 = -1/RC$ must compensate the pole p_1 ($z_1 = p_1$).
The two new poles are found from the expression:

$$p^2RC(C_{e2}+C_{f2}+C_{o1})+p\{2C+C_{e2}+C_{f2}+C_{o1}+ +RC(1-\alpha_2)g_{fe2}+(RC/R_1)\}+(1-\alpha_2)g_{fe2}+(1/R_1) = 0,$$

which gives:

$$p_o = \frac{(1-\alpha_2)g_{fe2}+(1/R_1)}{2C+C_{e2}+C_{f2}+C_{o1}+RC\{(1-\alpha_2)g_{fe2}+(1/R_1)\}},$$

$$\simeq \frac{(1-\alpha_2)g_{fe2}+(1/R_1)}{2C},$$

$$= \frac{1}{2C}\left(\frac{g_{fe2}}{h_{fe2}}+\frac{1}{R_1}\right),$$

$$= \frac{1}{2C}\left(\frac{1}{R_{i1}}+\frac{1}{R_1}\right) = \frac{R_1+R_{i1}}{2CR_1R_{i1}}, \qquad \ldots(25)$$

and

$$p_2' = \frac{-2C+C_{e2}+C_{f2}+C_{o1}+RC\{(1-\alpha_2)g_{fe2}+(1/R_1)\}}{RC(C_{e2}+C_{f2}+C_{o1})}$$

$$\simeq \frac{-2}{RC_{e2}} = \frac{-2\omega_{(hfb)2}}{Rg_{fe2}}. \qquad \ldots(26)$$

Economical 3W record-player amplifier

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UDC 621.375.4.026.441:681.84

A 3W transistor amplifier for use in record-players with cartridges giving an output of 300mV at 1cm/s is described. The circuit may be adapted to include comprehensive tone control.

INTRODUCTION

The amplifier shown in Fig. 1 is suitable for use with cartridges giving an output of 300mV at 1cm/s, and may be adapted to include comprehensive tone control (see Fig. 4). The circuit uses a complementary output pair of one AC176 and one AC128 transistor, a BC107 driver transistor and a BC148 transistor.

CIRCUIT DESCRIPTION

A crystal pick-up requires a high load (1 to 2MΩ) if the bass response is to be adequate. A simple way to provide this load, and at the same time minimise gain spreads, is to apply feedback in series with the input. This technique is used in this amplifier.

Transistor TR_1 is an emitter follower supplying the driver transistor TR_2. Because of the large amount of feedback used in the circuit, the output transistors, TR_3 and TR_4, can have simple resistive bias. The output voltage is divided by resistors R_{11} and R_{12} and fed back to the input. The network C_4 and R_{10} forms a simple treble cut control.

The loudspeaker and capacitor C_6 are interchanged with respect to their conventional positions to provide a low-voltage supply for the collector of transistor TR_1, and also a point relatively free from a.c. signals from which d.c. feedback can be taken. The output mid-point voltage is compared with the base voltage of transistor TR_1 by the potential divider comprising resistors R_2, R_3 and R_4. Although the voltage is taken from a nominally d.c. point, decoupling is still required to remove low frequencies.

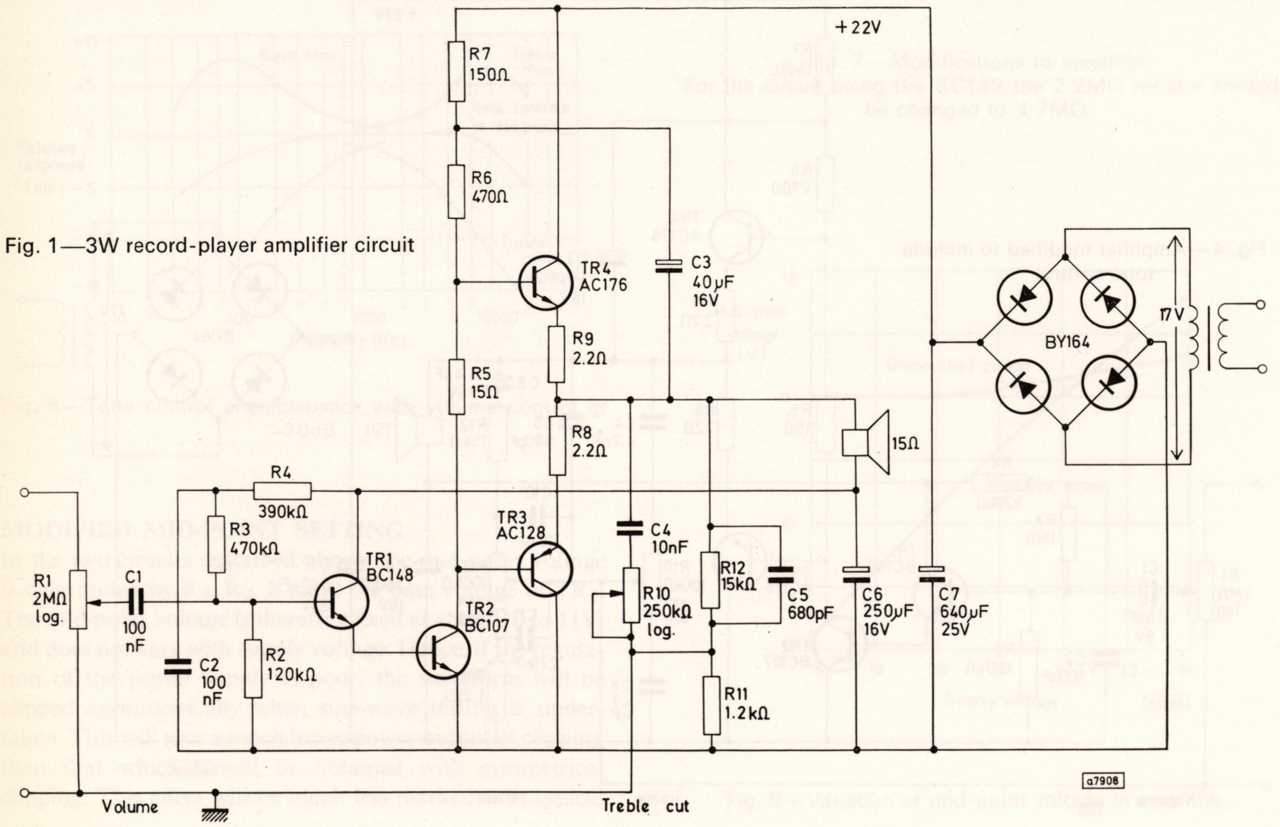


Fig. 1—3W record-player amplifier circuit

Performance

Output power	3	W r.m.s.
Sensitivity for full output	600	mV
Input resistance:		
with volume control at maximum	660	kΩ
with volume control at minimum	2	MΩ
Feedback, depending on position of volume control, up to	25	dB
Distortion at 2W output:		
with volume control at maximum	0·4	%
with volume control at −10dB	2	%
Quiescent current	20	mA
Total current at 3W output	210	mA

Fig. 2 shows the variation in bass response with volume control setting, resulting from the variation in input resistance. It should be noted that the circuit given in Fig. 2 representing the pick-up was used to obtain these curves.

Fig. 3 shows the variation of distortion with output power. With the volume control at maximum setting the feedback is high and the distortion low. However, at intermediate settings of the volume control the feedback is reduced, because of the increase in source impedance, and the distortion is higher.

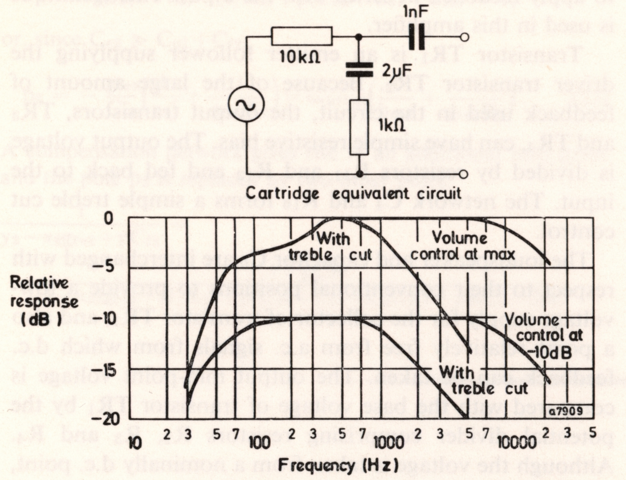


Fig. 2—Frequency response of amplifier, with the cartridge equivalent circuit as used

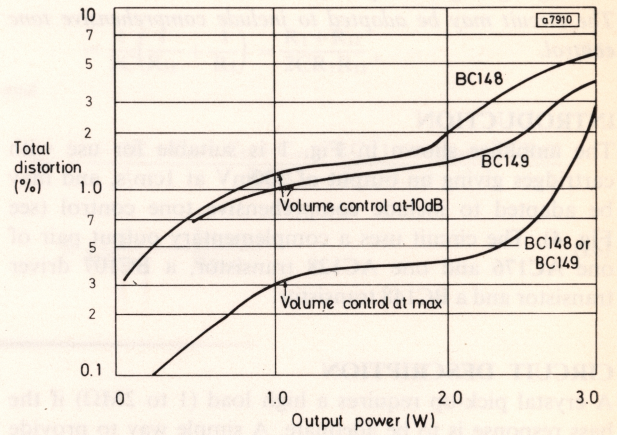
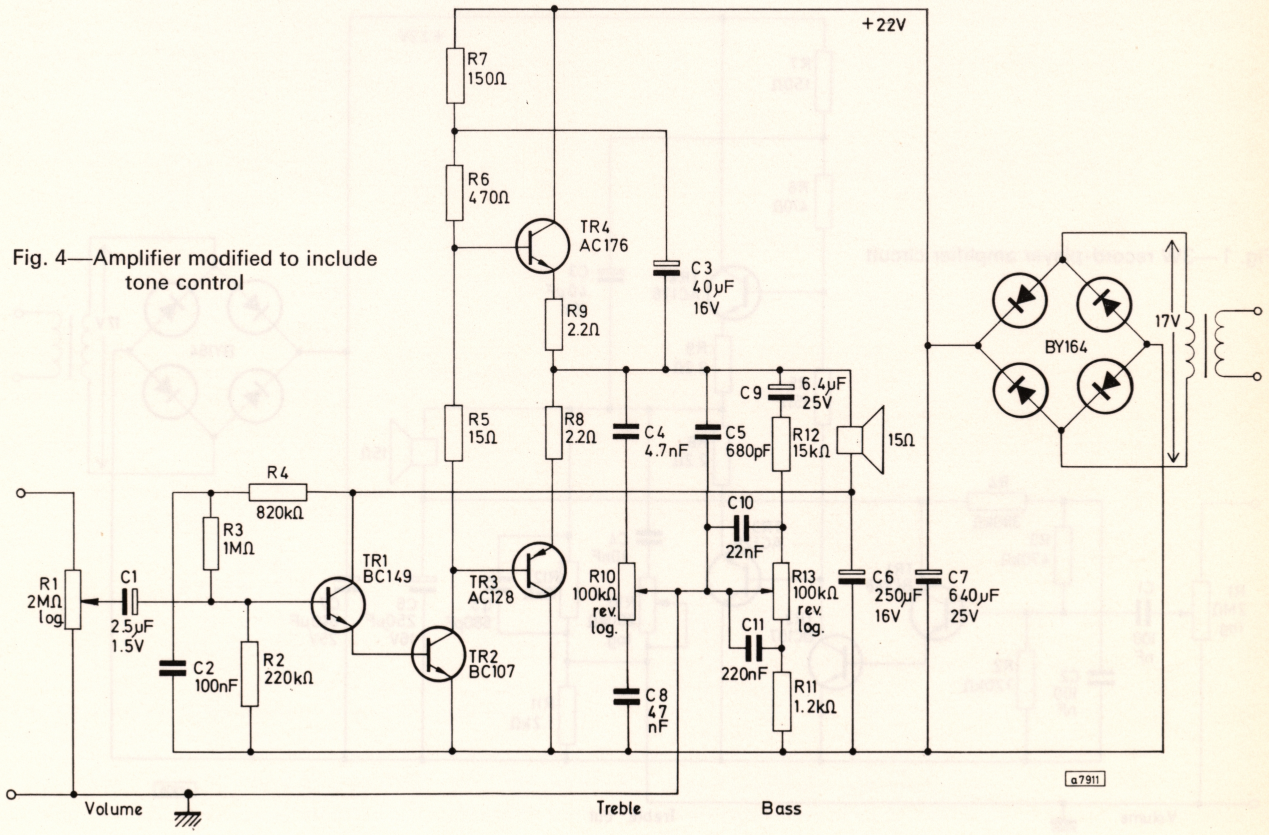


Fig. 3—Variation of total harmonic distortion with output power for the basic amplifier and the modified circuit

Fig. 4—Amplifier modified to include tone control



Circuit adapted to include comprehensive tone control

The feedback circuit may be modified to give bass and treble cut and boost controls, as shown in Fig. 4.

The input transistor TR$_1$ is a BC149, since this device gives a useful improvement in bass response and also in distortion (see Fig. 3). The tone control characteristics with volume control at maximum and at −10dB are shown in Figs. 5 and 6. The value of capacitor C$_1$ is increased to ensure low-frequency stability with bass boost applied. Capacitor C$_9$ is included to block d.c. from the bass control, and so prevent noisy operation.

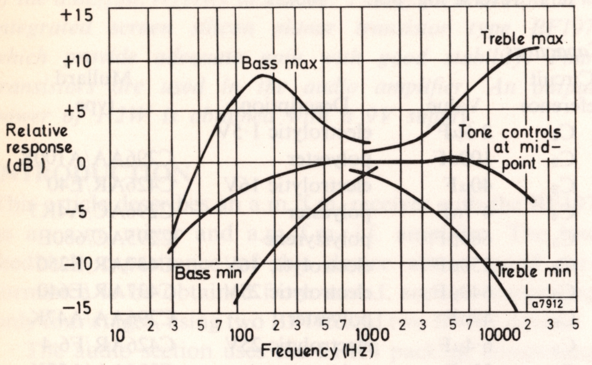


Fig. 5—Tone control characteristics with volume control at maximum

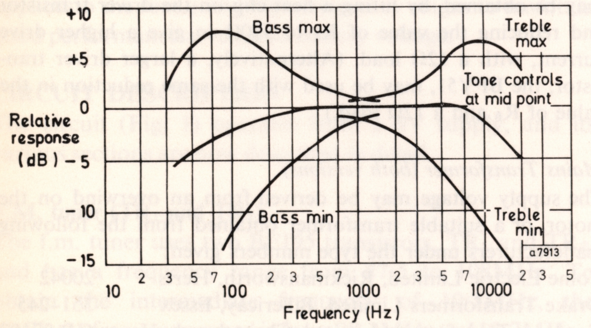


Fig. 6—Tone control characteristics with volume control at −10dB

MODIFIED MID-POINT SETTING

In the two circuits described above, the mid-point voltage is determined by R$_2$, R$_3$, R$_4$ and the base voltage of TR$_1$. The mid-point voltage is therefore fixed at about 10 to 11V, and does not vary with supply voltage. Hence, if the regulation of the power supply is poor, the waveform will be clipped asymmetrically when sine-wave testing is undertaken. This will give a much lower power output at clipping than that which would be obtained with symmetrical clipping. This effect will be much less marked with typical speech and music drive where the mean current, and hence the supply voltage drop, is much lower than when sine-wave testing.

To obtain symmetrical clipping under all conditions it is necessary for the mid-point voltage to remain at approximately half the line voltage. This is achieved as shown in Fig. 7.

In this circuit, the mid-point is determined by the preset resistor and the base current of TR$_2$, which is, of course, the collector current of TR$_1$. It is necessary to use a preset resistor because of the spread in h_{FE} of TR$_2$. Fig. 8 shows the variation of mid-point voltage in the original and modified circuits.

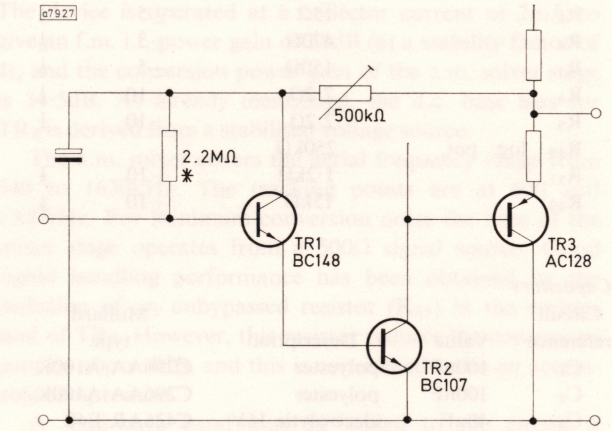


Fig. 7—Modifications to amplifier
*For the circuit using the BC149 the 2·2MΩ resistor should be changed to 4·7MΩ

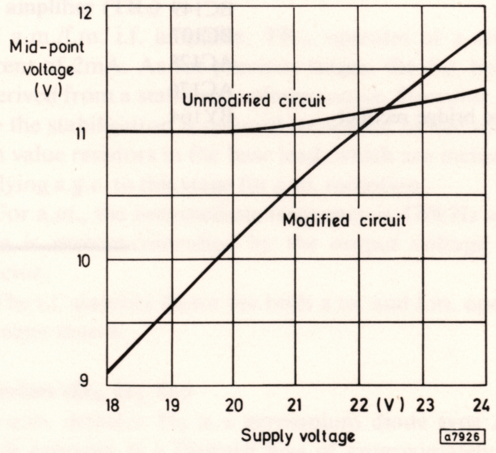


Fig. 8—Variation of mid-point voltage in amplifier

COMPONENTS

Components for basic version of amplifier

Transistors and Rectifier

Circuit reference	Mullard type
TR$_1$	BC148
TR$_2$	BC107
TR$_3$	AC128
TR$_4$	AC176
Full-wave bridge rectifier	BY164

Resistors

Circuit reference		Value	Tolerance (%)	Power rating (W)
R$_1$	log. pot.	2MΩ		
R$_2$		120kΩ	±5	$\frac{1}{8}$
R$_3$		470kΩ	±5	$\frac{1}{8}$
R$_4$		390kΩ	±5	$\frac{1}{8}$
R$_5$		15Ω	±5	$\frac{1}{8}$
R$_6$		470Ω	±5	$\frac{1}{2}$
R$_7$		150Ω	±5	$\frac{1}{2}$
R$_8$		2·2Ω	±10	$\frac{1}{4}$
R$_9$		2·2Ω	±10	$\frac{1}{4}$
R$_{10}$	log. pot.	250kΩ		
R$_{11}$		1·2kΩ	±10	$\frac{1}{8}$
R$_{12}$		15kΩ	±10	$\frac{1}{8}$

Capacitors

Circuit reference	Value	Description	Mullard type
C$_1$	100nF	polyester	C296AA/A100K
C$_2$	100nF	polyester	C296AA/A100K
C$_3$	40μF	electrolytic 16V	C426AR/E40
C$_4$	10nF	polyester	C296AA/A10K
C$_5$	680pF	polystyrene	C295AC/680E
C$_6$	250μF	electrolytic 16V	C437AR/E250
C$_7$	640μF	electrolytic 25V	C437AR/F640

Components for version including comprehensive tone control

Transistors and Rectifier

Circuit reference	Mullard type
TR$_1$	BC149
TR$_2$	BC107
TR$_3$	AC128
TR$_4$	AC176
Full-wave bridge rectifier	BY164

Resistors

Circuit reference		Value	Tolerance (%)	Power rating (W)
R$_1$	log. pot.	2MΩ		
R$_2$		220kΩ	±5	$\frac{1}{8}$
R$_3$		1MΩ	±5	$\frac{1}{8}$
R$_4$		820kΩ	±5	$\frac{1}{8}$
R$_5$		15Ω	±5	$\frac{1}{8}$
R$_6$		470Ω	±5	$\frac{1}{2}$
R$_7$		150Ω	±5	$\frac{1}{2}$
R$_8$		2·2Ω	±10	$\frac{1}{4}$
R$_9$		2·2Ω	±10	$\frac{1}{4}$
R$_{10}$	reverse log. pot.	100kΩ		
R$_{11}$		1·2kΩ	±10	$\frac{1}{8}$
R$_{12}$		15kΩ	±10	$\frac{1}{8}$
R$_{13}$	reverse log. pot.	100kΩ		

Capacitors

Circuit reference	Value	Description	Mullard type
C$_1$	2·5μF	electrolytic 1·5V	
C$_2$	100nF	polyester	C296AA/A100K
C$_3$	40μF	electrolytic 16V	C426AR/E40
C$_4$	4·7nF	polyester	C296AC/A4K7
C$_5$	680pF	polystyrene	C295AC/680E
C$_6$	250μF	electrolytic 16V	C437AR/E250
C$_7$	640μF	electrolytic 25V	C437AR/F640
C$_8$	47nF	polyester	C296AA/A47K
C$_9$	6·4μF	electrolytic 25V	C426AR/F6·4
C$_{10}$	22nF	polyester	C296AA/A22K
C$_{11}$	220nF	polyester	C296AA/A220K

Heatsinks (both versions)

Each output transistor should be mounted on a 1·5mm (16 gauge) bright aluminium heatsink with an area of 30cm². In the circuit shown the driver transistor does not require a heatsink. However, an increase in output power (3W at clipping) may be obtained, by fitting a heat clip on the driver transistor and reducing the value of R$_6$ to 330Ω to give a higher drive current, with a 12Ω load. (Alternatively, a larger driver transistor, the BFY51, may be used with the same reduction in the value of R$_6$ and a 12Ω load.)

Mains Transformer (both versions)

The supply voltage may be derived from an overwind on the motor, or a suitable transformer obtained from the following manufacturers under the type numbers given:

Colne Electric Limited, Rickmansworth, Herts	20042
Drake Transformers Limited, Billericay, Essex	351–245
Gardners Transformers Limited, Christchurch, Hants	GR 97182
Parmeko Limited, Aylestone Park, Leicester	P 3203

Portable a.m./f.m. radio receiver

A. Garskamp
Central Application Laboratory, Philips, Eindhoven

UDC 621.396.62[621.376.2][621.376.3]—182.4

Four transistors only are required in the r.f. and i.f. stages of the a.m./f.m. receiver described. Two of these are the new integrated screen silicon planar transistor type BF197 which provide adequate gain with good stability. Four transistors are used in the audio amplifier. An output power of 1·2W is obtained with a 9V supply.

INTRODUCTION

This article describes an a.m./f.m. receiver with the BF197 as an a.m. mixer and a.m./f.m. i.f. amplifier. The low feedback capacitance of this device allows good performance to be obtained from an h.f. section comprising only four stages, using two BF195 and two BF197 devices.

The audio section uses the LFK4 package comprising four transistors; that is, an AC127/AC128 matched complementary output pair, together with an AC128 driver and an AC127 pre-amplifier.

An asymmetric voltage-dependent resistor is used to stabilise the base voltage of the BF197 transistors, so that normal d.c. current gain spreads can be tolerated and gain grouping is unnecessary. The stabilised base voltage is also applied to the remaining high-frequency stages to maintain good performance at reduced battery voltage.

CIRCUIT DESCRIPTION

The circuit (Fig. 1) operates from a 9V supply, and its various sections are now described in detail.

F.M. tuner (TR$_1$ and TR$_2$)

The f.m. tuner uses two BF195 transistors, TR$_1$ and TR$_2$, and has a frequency range from 87·5 to 108MHz. To obtain the intermediate frequency of 10·7MHz, the oscillator frequency range is from 98·2MHz to 118·7MHz.

The f.m. tuner is conventional in design. For a.m. reception, the first r.f. stage operates as an a.g.c. amplifier to give sufficient control energy to drive the a.g.c. damping diode D$_2$, connected across the primary of the first a.m. i.f. bandpass filter. Both stages operate at a collector current of 1mA, and the current is stabilised against supply voltage variations by means of an asymmetric voltage-dependent resistor. The gain of the r.f. section is therefore substantially constant, and oscillator frequency drift minimised (less than 10kHz/V), at decreased battery voltage.

The fixed tuned input circuit is designed for a balanced aerial with a real impedance of 300Ω, or an unbalanced 75Ω aerial using half of the input winding.

For a.m. reception, the mixer/oscillator stage is switched off by means of switch S$_B$.

A.M. mixer and first f.m. i.f. stage (TR$_3$)

The feedback capacitance of the BF197 is typically 0·3pF at a collector current of 1mA and a collector-emitter voltage of 10V. This is an improvement of approximately three times over that of conventional h.f. transistors. The device is operated at a collector current of 2mA to give an f.m. i.f. power gain of 28dB (at a stability factor of 4), and the conversion power gain of the a.m. mixer stage is 34·5dB. As already mentioned, the d.c. base bias for TR$_3$ is derived from a stabilised voltage source.

The a.m. mixer covers the aerial frequency range from 540 to 1630kHz. The tracking points are at 600 and 1300kHz. For minimum conversion noise the base of the mixer stage operates from a 500Ω signal source. Good signal handling performance has been obtained by the inclusion of an unbypassed resistor (R$_{11}$) in the emitter lead of TR$_3$. However, this resistor reduces the conversion gain by about 4dB, and this is considered to be an acceptable compromise.

A long-wave band may be added to the circuit if required and details of the necessary coils are included at the end of the article; extra switching would also be required.

The f.m. intermediate frequency is 10·7MHz. To avoid a reduction in gain as a result of the presence of R$_{11}$ in the emitter lead of TR$_3$, the i.f. input signal is applied between base and emitter of TR$_3$. The i.f. stability factor of this stage is greater than 4.

I.F. amplifier (TR$_4$)

The a.m./f.m. i.f. amplifier, TR$_4$, operates at a collector current of 2mA. As for previous stages, the d.c. base bias is derived from a stabilised voltage source. However, in this case the stabilisation is reduced somewhat by the relatively high value resistors in the base lead, which are included for applying a.g.c. to this stage for a.m. reception.

For a.m., the intermediate frequency is 470kHz and the stage is reverse-controlled by the output voltage of the detector.

The i.f. stability factor for both a.m. and f.m. operation is greater than 4.

Detectors (D$_3$, D$_4$, D$_5$)

The a.m. detector D$_3$ is a germanium diode type AA119 which operates at a forward bias of approximately 50mV to improve the detector efficiency at small signal levels. For handling a modulation depth of 80%, the source impedance of the detector must be 10kΩ, requiring a

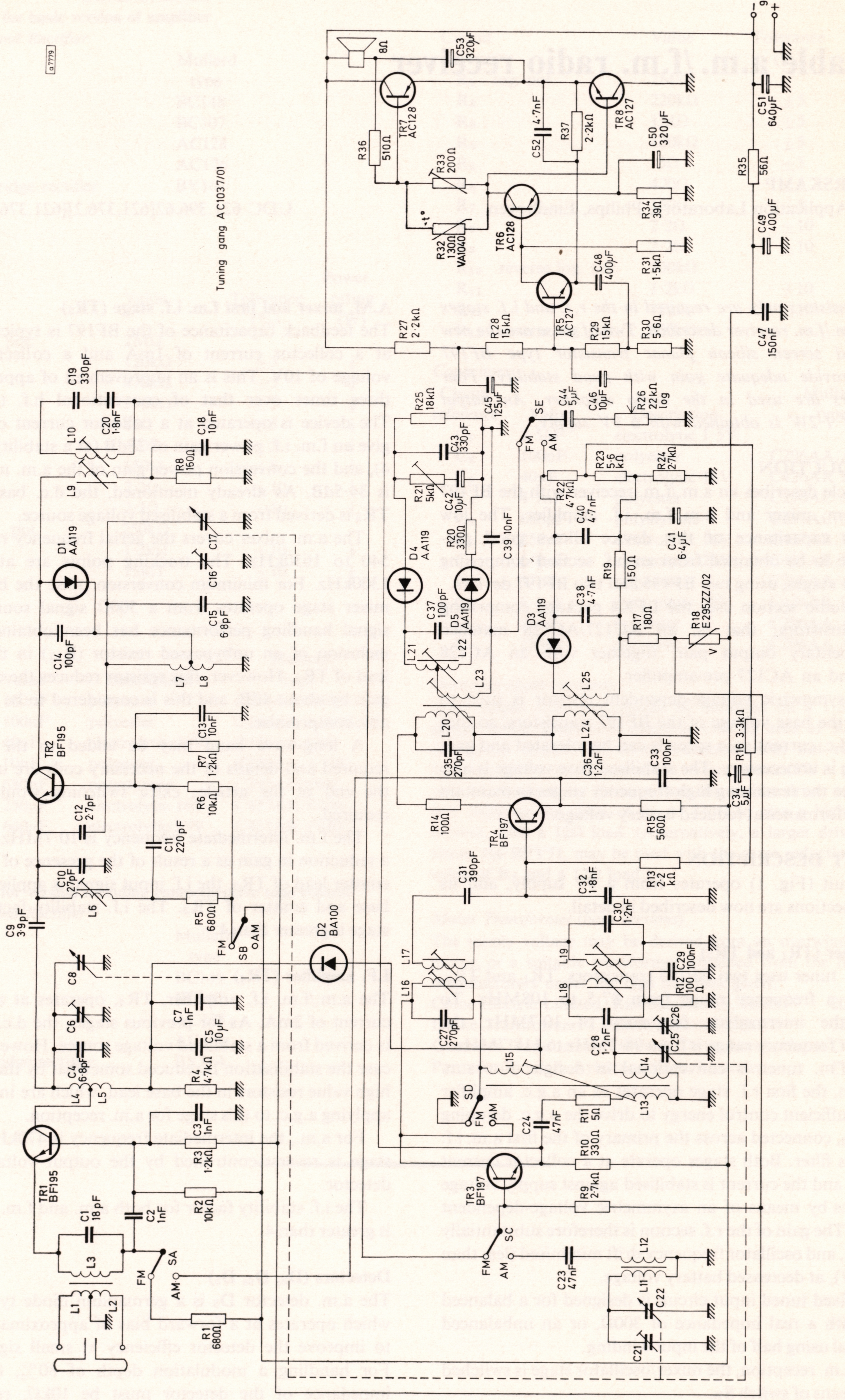

a7779
Tuning gang AC1037/01
8Ω
C53 320µF
TR7 AC128
R36 510Ω
R33 200Ω
-t°
R32 130Ω VA1040
TR6 AC128
C52 4·7nF
R37 2·2kΩ
TR8 AC127
C50 320µF
R34 39Ω
C48 400µF
R31 1·5kΩ
TR5 AC127
R27 2·2kΩ
R28 15kΩ
R29 15kΩ
R30 5·6Ω
9V
−
+
C51 640µF
R35 56Ω
C49 400µF
C47 150nF
C19 330pF
C20 1·8nF
L10
L9
C18 10nF
R8 160Ω
D1 AA119
C17
C16
C15 6·8pF
C14 100pF
L7
L8
C13 10nF
R7 1·2kΩ
TR2 BF195
R25 18kΩ
C45 125µF
C43 330pF
R21 5kΩ
C42 10µF
R20 330Ω
C39 10nF
D4 AA119
D5 AA119
C37 100pF
L21
L22
L23
L20
C35 270pF
SE
FM
AM
C44 5µF
C46 10µF
R26 22kΩ log
R22 4·7kΩ
R23 5·6 kΩ
R24 27kΩ
C40 4·7nF
C41 6·4µF
R19 150Ω
D3 AA119
C38 4·7nF
R17 180Ω
R18 E295ZZ/02
V
L25
L24
C36 1·2nF
C33 100nF
R16 3·3kΩ
C34 5µF
C12 2·7pF
R6 10kΩ
C11 220pF
C10 27pF
L6
R5 680Ω
C9 3·9pF
FM
SB
AM
C8
D2 BA100
C7 1nF
C6
C5 10µF
C4 6·8pF
L4
L5
R4 4·7kΩ
C3 1nF
R3 1·2kΩ
TR1 BF195
C1 18pF
L3
C2 1nF
R2 10kΩ
FM
SA
AM
L1
L2
R1 680Ω
R14 100Ω
TR4 BF197
R15 560Ω
C31 390pF
R13 2·2 kΩ
C32 1·8nF
C30 1·2nF
L17
L16
C27 270pF
L19
L18
C29 100nF
R12 100 Ω
C28 1·2nF
C26
C25
L15
L14
SD
FM
AM
C24 47nF
R11 5Ω
L13
R10 330Ω
TR3 BF197
R9 2·7kΩ
SC
FM
AM
C23 47nF
L12
L11
C22
C21

Fig. 1—Complete receiver.

tapping ratio of 0·5 on a tuned circuit with dynamic impedance of about 40kΩ ($Q_o = 145$; tuning capacitor 1·2nF). With a tapping ratio of 0·5 and a detector efficiency of 80%, the reflected detector damping at the top of the tuned circuit is 25kΩ which, together with the damping of the tuned circuit and the transistor, gives a total collector damping of 13·5kΩ. To obtain sufficient i.f. output power from the reverse controlled i.f. transistor, especially at the end of gain control, the collector load of 13·5kΩ provides power matching for an emitter current of 350µA for TR_4.

The f.m. detector is a conventional ratio detector using a matched pair of diodes, D_4 and D_5, type 2–AA119.

A.G.C. circuit (a.m.)

The a.g.c. system consists of two loops, one controlling the amplification of the i.f. transistor TR_4 and the other the damping of the primary L_{18} of the first a.m. i.f. bandpass filter.

Since the high gain of the mixer stage makes a high degree of control by the damping diode necessary, a separate a.g.c. amplifier delivering sufficient drive for this diode is required. The effect of this loop is to prevent the i.f. transistor TR_4 from becoming over-driven before the maximum permissible aerial voltage at the input of the mixer transistor is reached. To obtain a good signal-to-noise ratio, especially with weak aerial signals, the control of the damping is delayed. The d.c. output voltage of the detector is applied to the base of TR_4, which is driven to a lower current (reverse control) for increasing aerial signals. Since TR_1 and TR_4 are connected in a long-tail pair configuration, the operating current of TR_1 increases as the emitter current of TR_4 decreases. The damping diode is forward biased by the collector current of TR_1.

With weak aerial signals, the collector currents of the two transistors are out of balance, so that if TR_4 operates at its nominal current 2mA, the collector current of TR_1 is zero. As the base bias of TR_1 is lower than that of TR_4, TR_1 becomes conductive only after a certain voltage delay. To ensure sufficiently low damping with weak signals, the damping diode is reverse biased by means of a voltage drop of 200mV developed across the collector resistor R_{12} of TR_3.

A.F. amplifier (TR_5 to TR_8)

The audio frequency amplifier uses four germanium transistors in the a.f. package LFK4. The output transistors TR_7 and TR_8 deliver an a.f. output power of 1·2W at a distortion level of 10% into a loudspeaker with an impedance of 8Ω.

The mid-point voltage of the output stage is 5V and is stabilised by d.c. feedback to the emitter of the a.f. pre-amplifier transistor TR_5.

To reduce gain spreads and distortion, 9dB of a.c. negative feedback is applied to the emitter of the pre-amplifier via resistors R_{30} and R_{37}.

The circuit can be used up to an ambient temperature of 45°C.

D.C. adjustment

The d.c. settings for nominal transistors are given in Table 1, together with total currents for the h.f. section and the entire receiver.

TABLE 1
Operating conditions

Transistor	Operating current I_C (mA) $V_s = 9V$	$V_s = 5{\cdot}5V$
TR_1	1·0	0·84
TR_2	1·0	0·84
TR_3	2·0	1·65
TR_4	2·0	1·4
TR_5	0·35	0·23
TR_6	7·7	4·9
TR_7	5·0	0·5
TR_8	5·0	0·5
H.F. section		
a.m.	6·5	4·3
f.m.	8·3	5·9
Total receiver		
a.m.	19·5	10·1
f.m.	21·3	11·6

For maximum output power (1·2W), the total current consumption is 160mA.

PERFORMANCE

Oscillator voltages

The oscillator voltages at the emitters of the mixer transistors at the centre of the relevant frequency ranges are:

a.m. operation: at $V_s = 9V$, 130mV;
at $V_s = 5{\cdot}5V$, 110mV
f.m. operation: at $V_s = 9V$, 200mV;
at $V_s = 5{\cdot}5V$, 175mV

Oscillator frequency shift

The oscillator frequency shifts as a function of battery voltage are:

a.m. operation: less than 150Hz/V at $f_{osc} =$ 2MHz
f.m. operation: less than 10kHz/V at $f_{osc} =$ 118MHz

Bandwidth and selectivity

For a.m. reception:

3dB bandwidth	5kHz
selectivity at 9kHz off-tune	25dB

(response of i.f. section only)

For f.m. reception:

3dB bandwidth	200kHz
selectivity at 300kHz off-tune	50dB

(overall response including ratio detector)

Sensitivity

The sensitivity levels of the a.m. circuit for an output power of 50mW into an 8Ω load are:

aerial input	92 µV/m
mixer/oscillator input	2·7µV
input of i.f. stage	145 µV
input of a.f. amplifier	5 mV

(These figures are for battery voltage = 9V, signal frequency = 1MHz, modulation depth = 30% and modulation frequency = 1kHz.)

The sensitivity levels of the f.m. circuit for an output power of 50mW into an 8Ω load are:

aerial e.m.f.	3·3µV
input of 1st i.f. stage	33 µV
input of 2nd i.f. stage	800 µV
input of a.f. amplifier	5 mV

(These figures are for battery voltage = 9V, signal frequency = 100MHz, frequency deviation = 15kHz, modulation frequency = 1kHz.)

A.G.C. and signal-to-noise ratio

Fig. 2 shows the signal and noise voltages at the input of the a.f. amplifier as a function of the a.m. input signal at the mixer base. Fig. 3 shows the signal and noise voltages at the input of the a.f. amplifier against the aerial e.m.f. for f.m. reception.

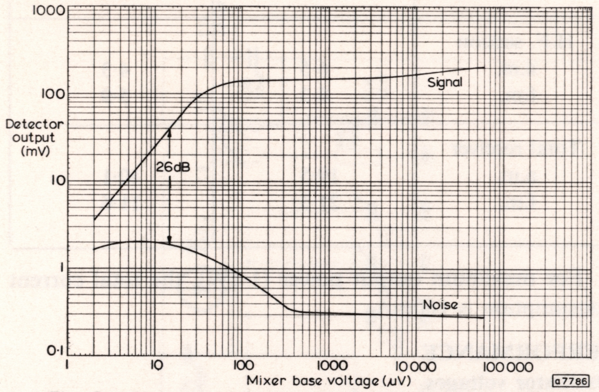


Fig. 2—Signal and noise voltages for a.m. reception
Signal frequency = 1MHz, modulation depth = 30%, modulation frequency = 1kHz

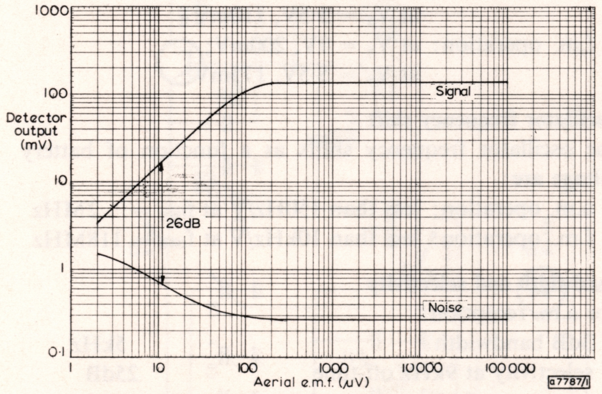


Fig. 3—Signal and noise voltages for f.m. reception.
Signal frequency = 100MHz, frequency deviation = 15kHz, modulation frequency = 1kHz

Frequency response

The 3dB frequency response of the a.f. amplifier is 100Hz to 20kHz.

Harmonic distortion

The total harmonic distortion is 4% at 800mW output, and 10% at 1·2W output.

HEATSINKS

For the AC128 output transistor a cooling clip only is required. For the AC127 a cooling clip mounted on a 1·5mm bright aluminium heatsink with an area of 12·5cm^2 is required.

COIL DATA

F.M. aerial coil

L_1, L_2	2·5 turns of 0·22mm diam. en.cu.
L_3	3 turns of 0·22mm diam. en.cu.; wound on a powder iron frame

F.M. insterstage coils

L_4+L_5	1·25+2·75 turns of 1mm diam. en.cu.; air-cored; internal coil diameter, 8mm

F.M. i.f. trap

L_6	9 turns of 0·3mm diam. en.cu.; wound on ferrite core

F.M. oscillator coils

L_7+L_8	3+1·5 turns of 1mm diam. en.cu.; air-cored; internal diameter 6mm

F.M. i.f. coils

L_9	12 turns of 36×0·03mm stranded wire, $Q_o = 120$
L_{10}	7 turns of 0·3mm en.cu., $Q_o = 90$; $kQ = 1·2$

Medium-wave aerial coils

L_{11}	80 turns of 36×0·03mm stranded wire wound along a length of 20mm (Q_o should be adjusted to 100 at 1MHz by addition of parallel damping)
L_{12}	4 turns of 36×0·03mm stranded wire; aerial rod, FX1247

Medium-wave oscillator coils

L_{13}	2 turns of 12×0·04mm stranded wire
L_{14}	110 turns of 12×0·04mm stranded wire, $Q_o = 145$ at 1MHz
L_{15}	5 turns of 12×0·04mm stranded wire

F.M. i.f. coils

L_{16}	7 turns of 36×0·03mm stranded wire, $Q_o = 105$
L_{17}	7 turns of 36×0·03mm stranded wire, $Q_o = 105$; $kQ = 1·2$

A.M. i.f. coils

L_{18}	70 turns of 12×0·04mm stranded wire, $Q_o = 150$
L_{19}	62 turns of 12×0·04mm stranded wire, $Q_o = 140$; $kQ = 1$

F.M. i.f. coils

L_{20}	7 turns of 36×0·03mm stranded wire, $Q_o = 110$
L_{21}	6 turns of 36×0·03mm stranded wire bifilar wound, $Q_o = 125$; $kQ = 0·7$
L_{22}	6 turns of 36×0·03mm stranded wire bifilar wound, $Q_o = 125$; $kQ = 0·7$
L_{23}	3 turns of 0·1mm en.cu.

A.M. i.f. coils

L_{24}	70 turns of 12×0·04mm stranded wire, $Q_o = 145$
L_{25}	35 turns of 12×0·04mm stranded wire

Coils L_9, L_{10} and L_{13} to L_{25} are wound with ferrite frames and cores.

A long-wave aerial coil may be added, if required, in the usual manner; 240 turns and 12 turns of 36×0·03mm stranded wire are required. It should be noted that switching for a long-wave band is not included in Fig. 1.